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PROGRAMMABLE IN-RASTER SYMBOL GENERATOR.(U)
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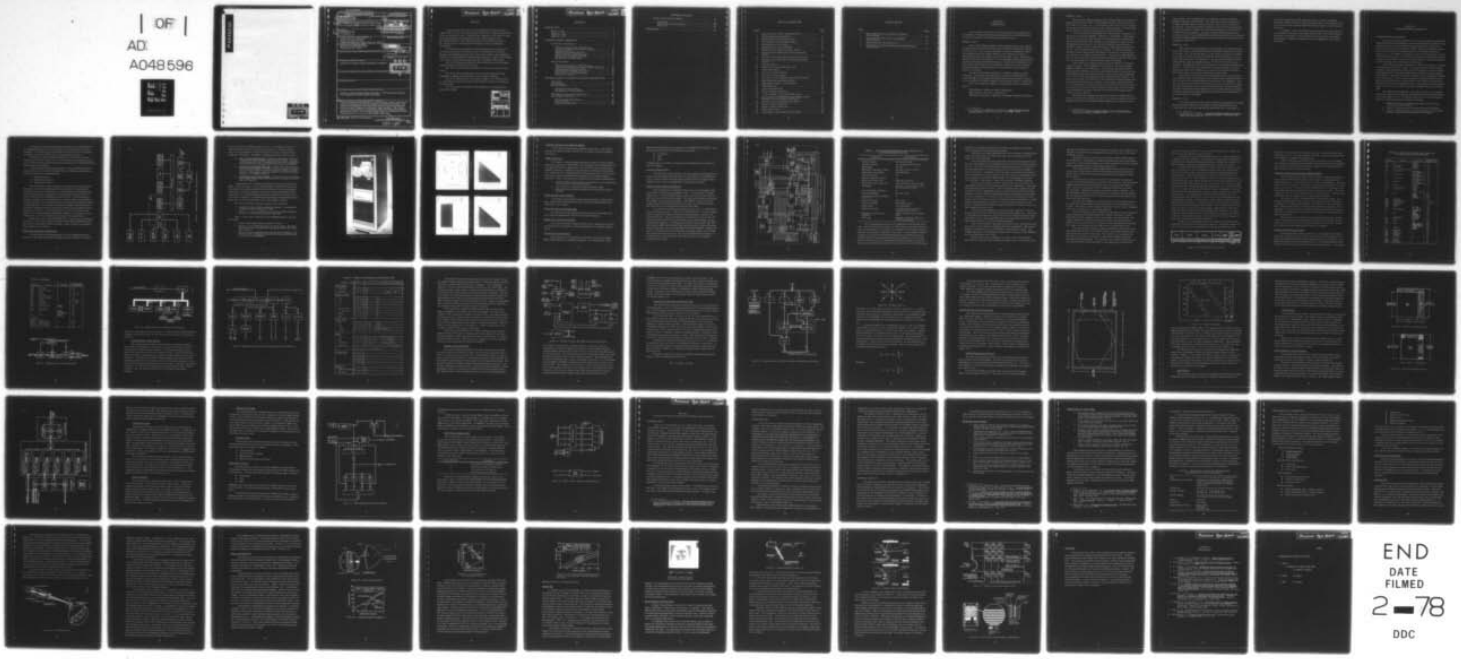

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: NADC 77259-30
2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): Programmable In-Raster Symbol Generator. Phase IV
5. TYPE OF REPORT & PERIOD COVERED: Final report, 1 Apr 75-Jun 76
6. PERFORMING ORG. REPORT NUMBER: HAC-P77-380, HAC-Ref-D4846
7. AUTHOR(s): G. Wolfson
8. CONTRACT OR GRANT NUMBER(s): N62269-75-C-0274
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Display Systems Laboratory, Hughes Aircraft Company, Centinela & Teale Sts., Culver City, Ca. 90230
10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS: Naval Air Development Center, Warminster, Pa. 18974
12. REPORT DATE: Nov 77
13. NUMBER OF PAGES: 61 (12) 66p.
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)
15. SECURITY CLASS. (of this report): Unclassified
15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Displays, Programmable Symbol Generator, Vertical Situation Display, Color Displays, In-raster Symbol Generator.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A programmable symbol generator, in-raster buffer refresh memory and software development station was designed, fabricated and tested. The system was developed to meet the Navy's needs for improved reliability vertical situation displays for advanced weapon systems. This report documents the last phase of a four phase study and development program sponsored by NADC. Also included in this report is a discussion of color requirements and a survey of color display technology.

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PREFACE

This final report covers the work accomplished during the period 1 April 1975 to 1 June 1976 under Contract N62269-75-C-0274, Programmable In-Raster Symbol Generator. This work was supported by the Naval Air Systems Command under the sponsorship of Mr. George Tsaparas and Mr. Russell Berthot. The program was under the technical direction of Mr. Harold Green of the Naval Air Development Center, Warminster, Pennsylvania.

The work was accomplished by the Display Systems and Human Factors Department under the direction of Mr. G. Wolfson who was Project Manager and contributed the material in the section entitled, The Application of Color to the Highly Reliable Vertical Display Systems. Special acknowledgement is given to the following individuals who contributed to the project.

Mr. J.R. Phelps performed the system integration task and provided technical guidance throughout the program.

Mr. M. Pruznick performed hardware checkout and detailed circuit design.

Mr. W.R. Byles performed the final circuit checkout and system integration in addition to providing the on-site support at NADC.

Mr. W.C. Hoffman, Mr. J.L. Heard, and Mr. H.D. Coulson acted as consultants to the program and provided valuable assistance in conduct of all major tasks.

Mr. J.W. Weber conducted a programming course for government personnel at NADC.

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SECTION 1
INTRODUCTION

This contract is the fourth in a series, initiated for the exploratory development of a Highly Reliable Vertical Display System (HRVDS) suitable for use by the Navy for the next generation attack aircraft.

PHASE I – 1972

Phase I of the Highly Reliable Vertical Display System was conducted during the period of June 1971 through July 1972 under Contract No. N62269-71-C-0510 ref 1. The results of the Phase I contract established the Operational Requirements for a highly reliable vertical display to be used in advanced Navy all weather attack aircraft in the 1980s. Also, Performance Requirements were established for a Vertical Display System capable of meeting the specified Operational Requirements. Finally, these Operational and Performance Requirements were translated into hardware mechanizations. Various candidate mechanizations were then traded off, and the optimum design was selected.

As part of the hardware tradeoffs, a reliability analysis was also conducted. That analysis identified the key elements contributing to the various MTBF's and quantified the MTBF improvements required to achieve an overall MTBF for a Highly Reliable Vertical Display System of 1000 hours.

This overall 1000 hour MTBF was apportioned to the three subunits as follows:

CRT Indicator – 4000 hours (CRT – 6000 hours)
Digital Symbol Generator – 10,000 hours
Digital Scan Converter – 2000 hours (accepting individual bit failures)

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1. J. L. Heard, H. J. Bjelland, E. Streeter. Highly Reliable Vertical Display System, Hughes Aircraft Co., P72-104R, 10/72.

PHASE II – 1973

Phase II of the Highly Reliable Vertical Display System was conducted during the period of November 1972 through November 1973 under Contract No. N62269-73-C-0333, ref. 2. The purpose of this study was to investigate the critical mechanization parameters for a Highly Reliable Vertical Display System with the overall goal of providing increased reliability.

The major element contributing to the CRT Indicator reliability is the cathode ray tube (Current MTBF = 3000 hours, Goal MTBF = 6000 hours). The effort covered under this contract was directed toward identifying the factors which determine CRT reliability and quantifying the effects of each, individually and collectively. To meet the viewability requirements in a 10,000 ft. lambert ambient, while operating the CRT within safe limits, the use of a contrast enhancement device is essential. A detailed analysis of alternate contrast enhancement techniques was performed and the results of the analysis were verified in the laboratory. A narrow band CRT phosphor, such as a P43, combined with both a matched bandwidth restrictive filter and two-way attenuation filter will provide the maximum contrast.

The second major subunit requiring increased MTBF is the digital symbol generator. The reliability goal to extend the currently estimated MTBF of 2700 hours to 10,000 hours. The technical approach to achieve this improved reliability is to make maximum utilization of large scale integrated (LSI) circuit fabrication techniques. This requires the development of a set of universal, programmable, LSI symbol generator modules. The effort covered under this contract was directed toward defining detailed symbol requirements (symbol size, position, scale change, speed of updating, etc.); partitioning the symbol generator into standard LSI modules and fabricating a partial symbol generator breadboard using small scale and medium scale integrated circuit logic elements to demonstrate the programmable symbol generator concept.

The third major subunit, the digital scan converter (DSC), utilizes about 1.8 million bits of solid state memory and requires various conversion techniques to provide standardized display outputs for the different sensor

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2. Anonymous. Phase II, Highly Reliable Vertical Display System, Hughes Aircraft Co., P73-482, 5/74.

input formats. The reliability goal is to extend the currently estimated MTBF of 1600 hours to 2000 hours. The dominant element contributing to the DSC reliability figure is the main memory, which for the most part is already LSI. The technical effort was therefore directed to the performance of a detailed analysis of PPI to TV conversion techniques to select the most reliable conversion approach. A memory address coordinate conversion technique using a P channel MOS Random Access Memory (RAM) was selected. A laboratory DSC breadboard system was used to evaluate the effects of video smoothing and bit failure.

PHASE III – 1974

Phase III of the Highly Reliable Vertical System was conducted during the period of March 1974 through December 1974 under Contract No. N62269-74-C-0342, ref 3. During this phase, a state-of-the-art CRT was evaluated in an effort to validate the CRT life model developed during Phase II, and to relate CRT performance to reliability. A special CRT was fabricated which contained four separate phosphor stripes, P1, P31, P43 and P44, on the faceplate. Extended life tests were performed at low, medium and high beam currents. The CRT life test indicated the existance of phosphor "burn-in" phenomenon which was not taken into account in the derivation of the phosphor life formula, and otherwise verified the formula itself.

The second major task performed during Phase III was the development and fabrication of key elements of the programmable symbol generation with the objective of providing improved performance and reliability. These key elements included the field refresh memory, memory input format logic, memory output format logic, post processor and master timing and control. The effort expended in the development of these key elements has resulted in significant achievements which should lead to both increased symbol generator performance and reliability.

PHASE IV – 1976

The tasks performed on the current contract, Programmable In-Raster Symbol Generator (Phase IV of the Highly Vertical Display System) and reported herein were concerned with the fabrication of the remaining key

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3. G. Wolfson, B. W. Keller. Breadboard Highly Reliable Vertical TV Display System, Phase III, Hughes Aircraft Co., P75-44R, 2/75.

elements of the programmable symbol generator, namely, the display processor, display generator and programmable panel, and integration of all of the elements into a working deliverable Programmable In-Raster Symbol Generator.

In addition, a study task was performed to assess the application of a color display presentation to the highly reliable VDS. This effort included a discussion of the utility of color for both video presentations and symbolic presentations in addition to providing a survey of applicable color display technology.

SECTION 2
IN RASTER SYMBOL GENERATOR

INTRODUCTION AND SUMMARY

The vertical situation display is one of the prime displays comprising AIMIS (Advanced Integrated Modular Instrumentation System), which is being designed to meet the instrumentation requirements of the advanced U.S. Navy all weather attack aircraft of the 1980s. The general baseline requirements for the VDS (Vertical Display System) were defined in the Phase I report, ref. 1. In addition to presenting video, derived from radar, infrared and electro-optical sensors, the VDS must provide an integrated presentation of flight data consisting of airspeed, heading, altitude, roll and pitch attitude, vertical velocity, angle of attack and command data.

Two symbol generation techniques, in-raster and stroke, were studied and compared in the Phase I report. It was shown that the stroke writing technique required high power linear deflection amplifiers but was a flexible and simple means of generating alphanumeric characters and high quality, large graphics. However, the stroke technique is not compatible with display of TV scan sensors. The in-raster technique of symbol generation is compatible with varied sensors, either directly or via digital scan conversion. Because of this overall compatibility with TV image display and better power efficiency, the in-raster symbol generation technique was selected for the VDS.

The exploratory development of the highly reliable Vertical Display System was further advanced during the Phase II effort and was documented in the final report, ref. 2. The specific objectives of the Phase II effort in the area of symbol generation included the following:

1. Define performance characteristics unique to the in-raster symbol generation technique.
2. Trade off alternate in-raster symbol generation techniques.
3. Initiate a detailed design of the recommended in-raster symbol generator approach and demonstrate its feasibility.

The programmable in-raster symbol generator was recommended for the VDS application based on its flexibility, growth potential and projected reliability. A detailed design was performed and documented, encompassing the Display Generator portion of the in-raster symbol generator.

During Phase III of the Highly Reliability Vertical Display System, documented in the final report, ref. 3, key elements of the symbol generator were developed and fabricated with the specific objective of providing improved performance and reliability.

A block diagram of the programmable in-raster symbol generator is shown in Figure 1. During the Phase III effort, the following elements were developed, fabricated and demonstrated.

1. Input format logic
2. Field refresh memory
3. Output format logic

The development of these elements, has resulted in advancements in the state-of-the-art that provide improved performance, increased pilot acceptance and increased reliability. The anticipated increased pilot acceptance results from the development of a unique intensity coding scheme to reduce visual breakup of symbology rotated in-raster. The improved performance results from the development of a memory address scrambling circuit which permits up to six-fold increase in the quantity of symbology capable of being displayed. The increased reliability anticipated will result from a significant reduction in the size of the field refresh memory without sacrificing display resolution. The overall architecture of the symbol generator suggests ease of maintainability through the addition, in a production system configuration, of built in test with fault isolation to the module level.

During the current study effort (Phase IV), reported herein, additional key elements of the highly reliable vertical situation display (HRVSD) symbol generator were purchased and/or developed. These elements are indicated by the shaded area in Figure 1.

Military Microcomputer (AN/UYK-30)

The MMC (Military Microcomputer) is a two's compliment general purpose microcomputer developed by Hughes Aircraft Company and adapted

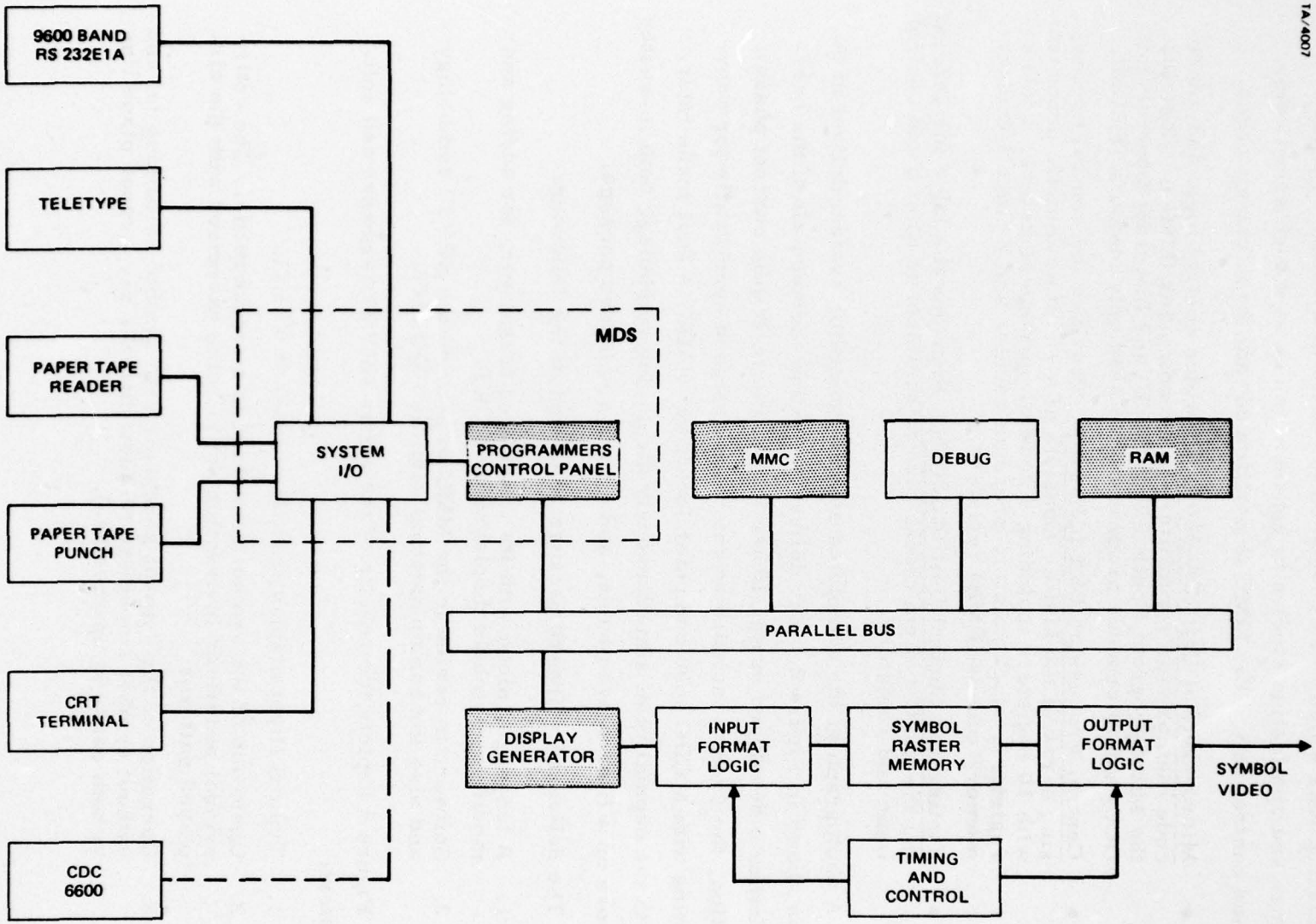


Figure 1. Programmable in-raster symbol generator.

for use as part of the HRVSD symbol generator. The MMC instruction set has 50 instructions which were chosen on the basis of avionics systems expe ience and application studies to enhance its use as a high speed computing and control unit. The MMC is partitioned into three circuit cards.

- Micro-Control Unit (CA-160). Provides control logic and microcode memory for the military microcomputer (MMC). Contains the Microprogram Control Unit (MCU) and Interrupt Control Unit (ICU) and microcode programmable read only memory (PROM).
- Central Processing Unit (CB-170). Provides the central processing array of the MMC. Consists of a 16 bit arithmetic processor with 10 registers including 4 general purpose registers, 2 index registers, stack pointer, program counter and 2 block I/O direct memory access (DMA) registers.
- Timing and Control Unit (CC-180). Provides the logic for generating the MMC system clock, plus miscellaneous timing and control logic and registers.

A photograph of the completed symbol generator system delivered to NADC is shown in Figure 2. The delivered system included all of the hardware elements developed during Phase III and Phase IV (the current phase). In addition, the system included an interface designed specifically for communicating with a CDC 6600 computer located at NADC, a dual mode interface with the capability of simultaneously displaying symbology both in-raster and stroke on a time shared basis, and a user's software package.

The delivered software package consisted of the following:

1. A language, along with its associated translator, for adding and modifying symbols displayed on a CRT.
2. Software to reside in the MMC to provide the HRVSD symbology and also for communicating with the CDC 6600.

Figure 3 depicts the results of the entire HRVSD hardware and software effort:

1. Typical flight display (525 line mode) at 0^{o} roll.
2. Operation of the symbol generator in a stroke mode. The entire symbol generator instruction set is being exercised with the displayed patterns.
3. Operation of the symbol generator with symbol smoothing (c) and without symbol smoothing (d) (note that the sky-ground plane line in both cases is unsmoothed).

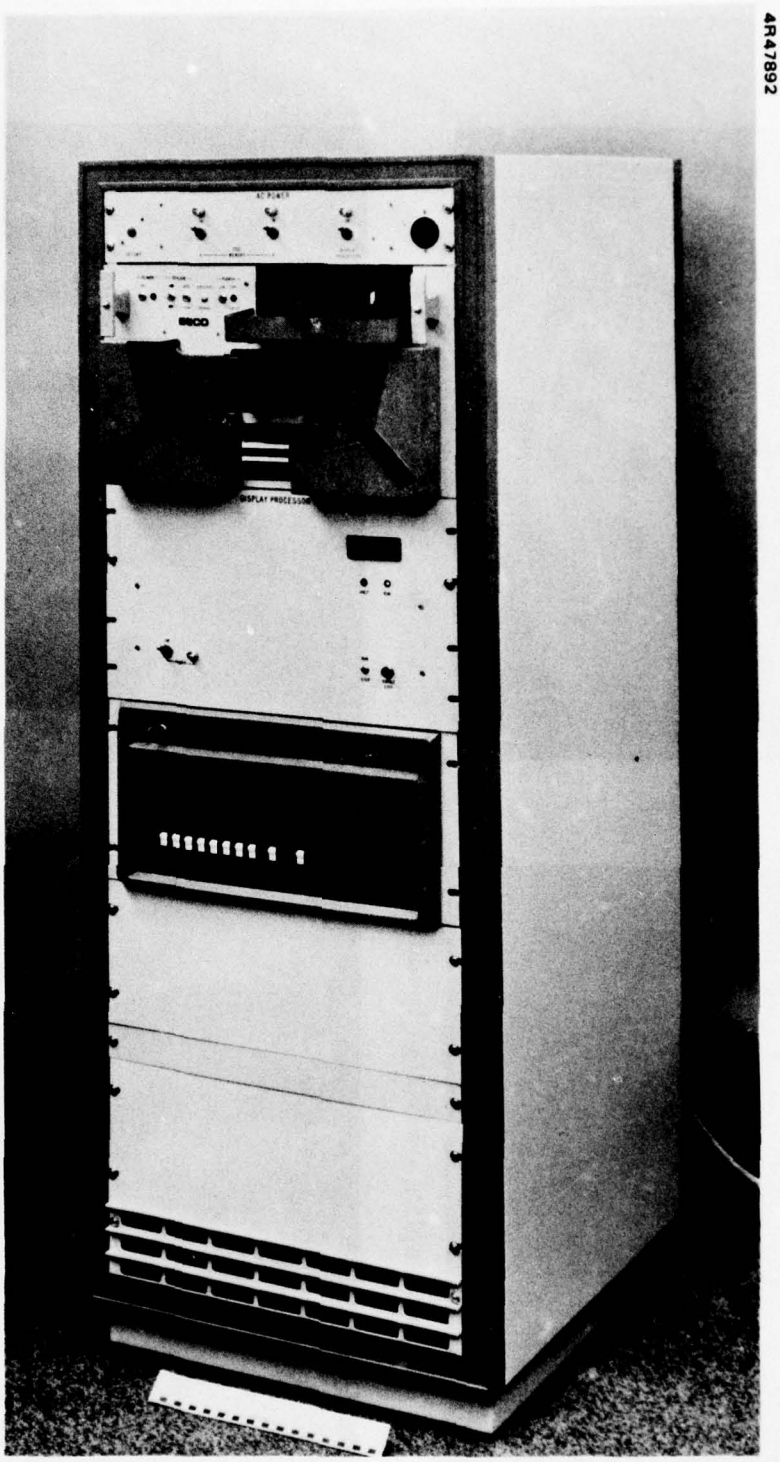
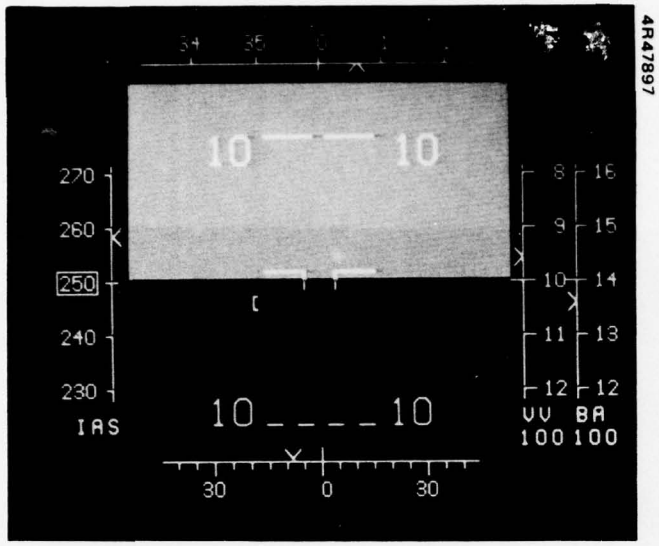
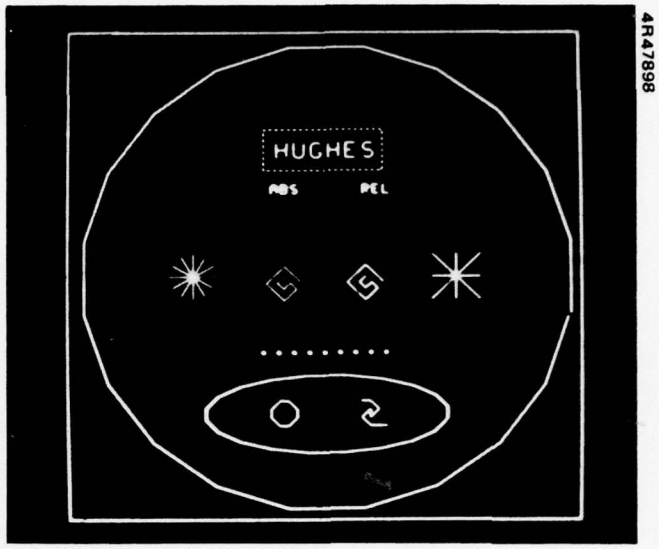


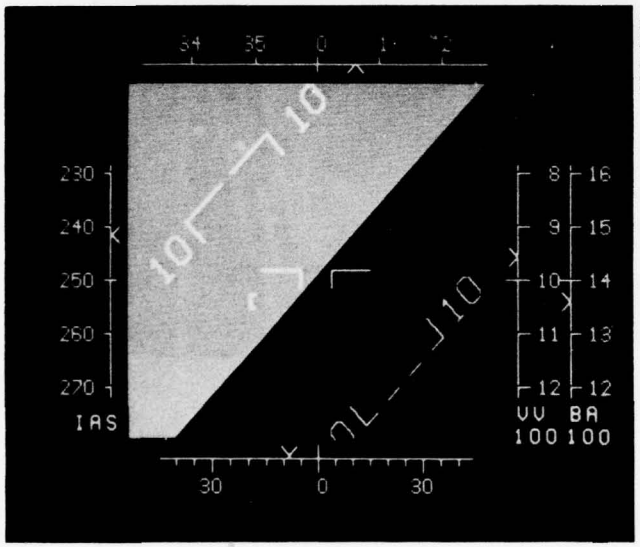
Figure 2. NADC symbol generator system.



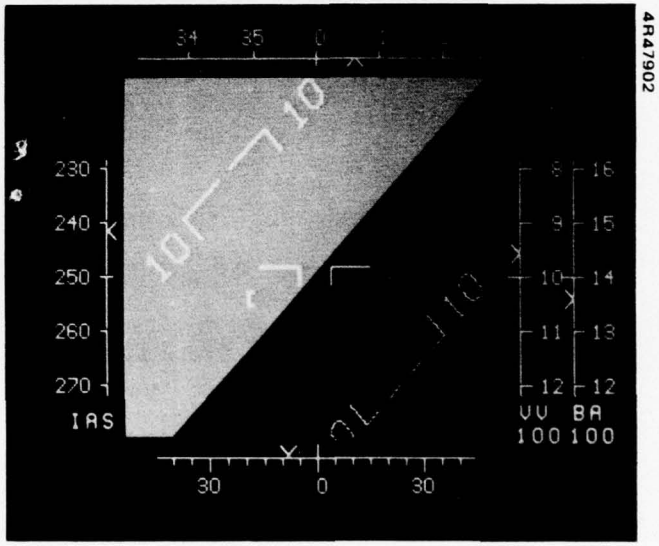
a. Flight display - 525 line mode.



b. Stroke symbology.



c. Flight display with symbol smoothing.



d. Flight display without symbol smoothing.

Figure 3. HRVSD hardware and software effort.

Controller Random Access Memory (RAM)

Two controller RAM modules (M190) are provided. Each module provides 4K words of 16 bits each for use as program storage and display list storage.

Display Generator

The Hughes developed display generator consists of a single sequential address generator controlled by a microcomputer-generated display list. The sequential address outputs may be D to A converted to provide analog deflection signals or encoded to form addresses for loading a refresh memory. The heart of the sequential address symbol generator is a pair of identical chain generator modules which output the X and Y symbol writing addresses. These chain generators perform three functions simultaneously:

1. They increment X and Y address accumulators in any of eight segment directions ("starburst" pattern)
2. They rotate this incremental chain through any angle
3. They displace the absolute location of the chain to any X and Y position.

Symbol Interface Buffer (SI-210)

The Symbol Interface Buffer module provides buffer storage for display symbol words and performs interface and housekeeping tasks for the symbol generator modules.

Symbol Executive Control (EC-220)

The Symbol Executive module decodes the symbol instructions and data words and supplies the Chain Generator control signals.

Symbol Chain Generator (CX-250)

Two of these identical modules provide X and Y addresses to the symbol refresh memory modules for storing symbol data in a television raster format.

Programmer's Control Panel

The Programmer's Control Panel (a purchased item) is an Intellec MDS 800 Microprocessor Development System. It is used both as a front

panel and peripheral interface controller for the MMC microcomputer. The purchased unit includes the following plug in modules:

- Front Panel
- CPU
- DMA

Additional spare card slots are provided in the MDS chassis for future system I/O modules.

MODULE DESCRIPTION

The following section contains a brief description and functional block diagram of each module provided under the current phase of the HRVSD program. Further details concerning these modules have been supplied under separate cover as part of an Operation and Maintenance Manual.

Military Microcomputer (AN/UYK-30)

The microprocessor controller (Figure 4) is a general purpose high speed military microcomputer (MMC) for use in a wide variety of avionics applications. The Intel Schottky bipolar 3000 series chip set forms the central core of the microcomputer design. The basic specifications and features of the MMC are summarized in Table 1. The MMC is configured on three modular boards: the Microcontrol Unit (CA-160); the Central Processing Unit (CB-170); and the Timing and Control Unit (CC-180).

The central processing array contains nine devices: 8 — 3002 Central Processing Elements and 1 — 3003 Carry Look-ahead Unit. Each processing element contains the required circuitry for implementing a 2-bit slice of a central processor. Thus, to construct a 16-bit machine, an array of 8 central processing element devices is required. This unit performs a variety of operations including: 2's complement arithmetic; logical AND, OR, NOT, and exclusive-NOR; increment and decrement; shift left or right; bit testing; and zero detection. The carry look-ahead unit speeds addition, shifting, and register testing operations by eliminating conventional ripple-carry through the central processing elements. The carry-out (CO) shown in Figure 4 is the output of the carry look-ahead chip rather than the most significant central processor chip.

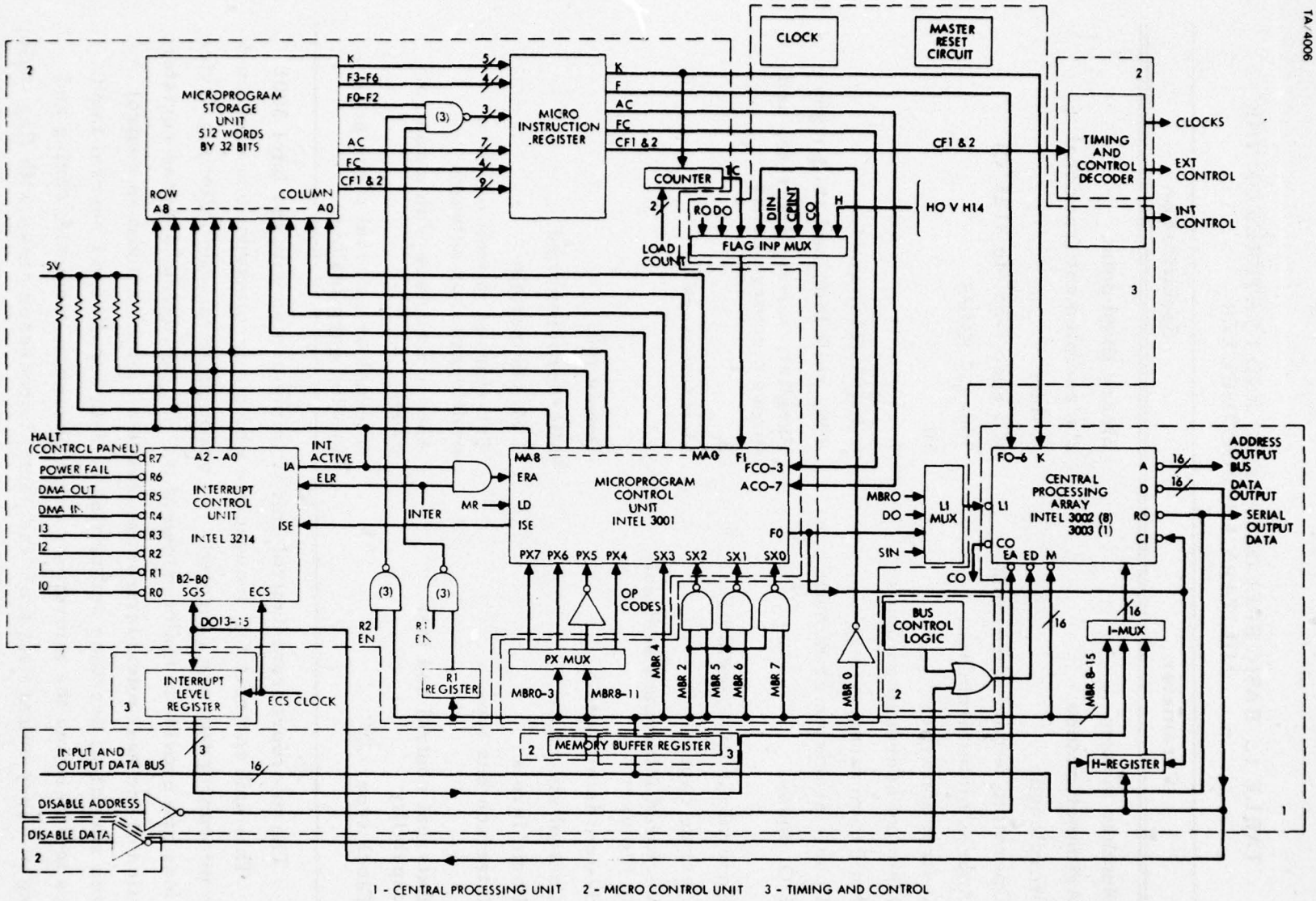


Figure 4. Microcomputer functional block diagram.

TABLE 1. BASIC SPECIFICATIONS AND FEATURES OF THE MILITARY MICROCOMPUTER

Parameter	Specification
Number system	Binary fixed point
Arithmetic Mode	2's complement fractional
Wordlength	16-bits
Operating temperature range	Mil spec (-55° to +125°C)
Approximate throughput	300-400 KOPS
Instruction types	50
Memory addressing modes	7
Maximum memory size	64K (65, 536) words
Double precision arithmetic	Add, shift left, and shift right
I/O modes	Parallel, serial, discrete, and direct memory access
General purpose registers	8
Nesting capability	Memory stack
Vectored interrupts available to the user	4
System interrupts	Power fail
Control sturcture	Microprogrammed
Logic levels	TTL compatible
Interface bus type	Tri-state to permit use in a multiprocessor network
External control and test capability	Able to interface with a control panel
Clock type	Internal or external clock generation permissible

The microprogram control unit is implemented with the Intel 3001 chip. This unit controls the sequence in which microinstructions contained in the microprogram are executed. To accomplish this the following device functions are provided: maintenance of the microprogram address register; selection of the next microinstruction based on the next address control function specified; decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence; saving and testing of carry output data from the central processor array with flag logic;

control of carry/shift input data to the central processing array with flag logic; and control of microprogram interrupts.

Multi-level interrupt capability for the microcomputer is implemented by the interrupt control unit (Intel 3214 chip). The interrupt control unit allows 8 levels of interrupt.

The microprogram storage unit stores the microinstructions that comprise the microprogram and is implemented with 4-512 x 8 read-only memory devices. The size of the storage unit is 512 words by 32 bits. The fields of the microinstruction word were highly coded to reduce the word widths as much as practical. In addition, sharing of code is used whenever possible to reduce the number of words required. The 512 words of microprogram memory is sufficient to allow the implementation of 50 instructions, 4 levels of user interrupt, a halt routine, a power fail interrupt, and DMA capability.

There are two primary interface busses of the microcomputer: the input/output data bus and the memory and I/O device address bus. Both input and output data use the same bus. This bi-directional bus configuration was selected because it substantially reduces the amount of interconnect cabling and buffer circuits required without significantly reducing the operating speed of the microcomputer. The address bus is used for accessing data in both memory and the I/O devices that are connected to the microcomputer. Enable signals indicate whether the address is to be used by the memory or I/O devices. Separate serial input and output data busses are provided, however, they constitute only two lines.

The left-in (LI) multiplexer selects one of four inputs for entry into the left input of the left-most chip of the central processing array. This input is normally used to enter the correct data into the vacated bit position when a right shift occurs. Serial input (SIN) data is entered LSB first into the left input during execution of the serial-input instruction.

The 16-bit H register augments the hardware of the central processing array and is used to speed the multiply and divide instructions. When multiplying a 16-bit number by a 16-bit number a 32-bit product results. The multiply operation is accomplished by performing a series of 32-bit additions and 1-bit right shifts of the result.

The purpose of the I multiplexer is to place one of three possible inputs onto the input bus of the central processing array. The sources of the

inputs to the multiplexer are the interrupt level register, the H register, and the address field of the word obtained from memory and stored in the memory buffer register.

Referring to Figure 4 there are two signals labeled disable address and disable data. The signals are buffered and both enter the central processing array. These control signals can be used to disable the tri-state address and data output busses of the central processing array.

The memory buffer register (MBR) buffers data transfers between the memory or I/O devices and the microcomputer to increase processor speed. It also allows the overlap of memory fetches for pipelined instruction execution.

The logic devices which surround the microprogram control unit increase its flexibility and permit a greater level of control. The Intel Microprogram Control Unit allows decoding of only one 4-bit op code field at a time. Thus if the instruction set to be implemented contains more than 16 instructions, additional decoding in successive steps is required. The PX multiplexer supplies op code information to the primary decode inputs of the microprogram control unit and allows two different op code groups to be decoded at different times.

The flag input multiplexer enters data from several possible sources throughout the microcomputer into the flag input of the microprogram control unit. This data is used to monitor operations, test for certain conditions, and assist in performing the operations required.

The 4-bit counter counts the number of steps that have been completed during execution of instructions requiring repetitive operations. These instructions include multiply, divide, serial input, and serial output. The counter reduces the amount of microcode necessary to implement these instructions and decreases their execution time by approximately 25 percent. The counter can be preset by the K field of the microinstruction word.

The interrupt level register contains the priority level of the current interrupt being executed. An identical register is provided inside the interrupt control unit for internal use only. The contents of the external 3-bit interrupt level register are stored in a stack by the central processing array when nesting interrupts. The interrupt level register and control unit are restored with the proper priority level by popping the stack after the

current interrupt is serviced. The value of the interrupt level register can also be set by the interrupt mask instruction

The purpose of the microinstruction register is to achieve pipelined execution of the microprogram. The register is 32 bits wide and buffers all output data bits from the microprogram memory. Without the register the microcomputer would operate approximately 30 to 40 percent slower.

The bits of the microinstruction register are used to control the central processing array, the microprogram control unit, and miscellaneous timing and control signals which are used internally and externally to the microcomputer. The microinstruction register is divided into fields as illustrated in Figure 5. The K field is a 5-bit field which is expanded into a 16-bit field before entry into the K input of the central processing array. By coding the K field 5 bits instead of 16 were required. The F field is a 7-bit function field that controls the operation performed by the central processing array. It includes the function code and the register designation. The function code from the microprogram memory directly controls the central processing array. The 7-bit address control field (AC) directly enters the microprogram control chip and is used to generate the next address for the microprogram memory. The 4-bit flag control field (FC) controls the flag input and output functions. Coded fields 1 and 2 (CF1 and CF2) are used to generate internal and external control signals. CF1 is 4 bits while CF2 consists of 5 bits, 2 of which are enable signals. Both fields are sent to the timing and control section of the microcomputer for decoding. The cotrol fields have been encoded to decrease the amount of microprogram memory required. These signals control various operations within the computer as well as the interfacing with external devices.

A clock circuit is provided as part of the basic microcomputer for generation of the periodic timing signals required. Provisions to allow use of an external clock for synchronization to special equipment are also

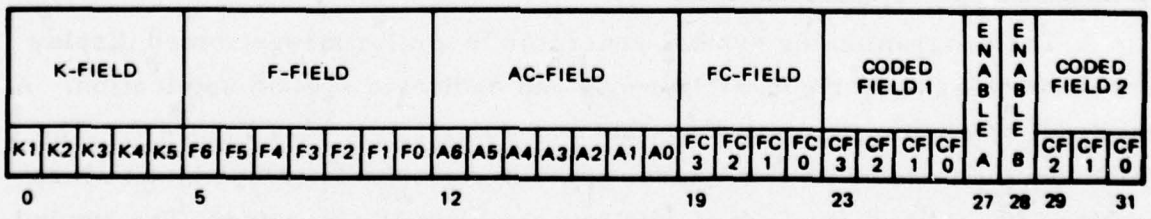


Figure 5. Microinstruction word format.

included. The internal clock is implemented with a crystal oscillator and a count-down circuit. The microcomputer includes a master reset circuit that will initialize the computer during power up.

Table 2 lists the instructions and their execution time on the MMC. The instruction execution times presented in the fourth column are calculated for memories with access time less than or equal to 150 nanoseconds and a basic machine cycle of 250 nanoseconds.

Controller Random Access Memory (RAM) (CM-190)

The microprocessor's main memory consists of 8K 16-bit words that can be used for data or instructions. The memory is partitioned into 4K modules (Figure 6). The memory utilizes a 4096 x 1 bit MOS chip. The memory cycle time is 750 nsec. The memory is volatile which requires a refresh cycle every 2 msec. In order to fit this configuration into a 16 pin pack, the 12 bit address lines are multiplexed into the chip 6 bits at a time. The least significant 6 bits are the row addresses and are latched first. Then the most significant 6 bits are enabled into the column address latches.

The 750 nsec cycle is divided into three 250 nsec time slots. The memory operation starts with a read or write request from the processor. The address is multiplexed in during the first 500 nsec. If the command is a write, data must be available during the second 250 nsec time slot. If the command is a read, data will be available during the last 250 nsec time slot. The transfer of data back to the processor is enabled by a data request line from the processor.

The refresh control consists of a refresh counter that times out the 2 msec refresh cycle and a refresh address counter that sequences through the 64 row addresses necessary for the refreshing of the memory. During the refresh cycle takes approximately 40 μsec to complete.

Programmable Symbol Generator

The programmable symbol generator is a microprogrammed display processor designed for general purpose and dedicated system application. A functional block diagram of the symbol generator is given in Figure 7. The MMC communicates with the symbol generator via the interface block which function is to control the flow of data into the symbol generator. The symbol

TABLE 2. INSTRUCTION EXECUTION TIMES OF THE MILITARY MICROCOMPUTER

Mnemonic	Instruction	Address Mode	Execution Time with a Fast Memory (μs)
ADD	Add	DIRECT INDEXED	1.5 2.0
ADI	Add Immediate	IMMEDIATE	1.25
AND	Logical AND	DIRECT INDEXED	1.75 2.25
BINC	Increment and Branch If Not Zero		2.25
BN	Branch Negative	RELATIVE REL. INDIRECT (+) REL. INDIRECT (-)	2.0 2.0 2.25
BNZ	Branch Not Zero	RELATIVE REL. INDIRECT (= 0) REL. INDIRECT (≠ 0)	2.0 2.0 2.25
BP	Branch Positive	RELATIVE REL. INDIRECT (= 0) REL. INDIRECT (≠ 0)	2.0 2.0 2.25
BZ	Branch Zero	RELATIVE REL. INDIRECT (= 0) REL. INDIRECT (≠ 0)	2.0 2.25 2.0
CMPR	Compare	DIRECT INDEXED	2.0 2.25
CPI	Compare Immediately	IMMEDIATE	2.0
DADD	Double Prec. Add	DIRECT INDEXED	2.25 3.0
DIV	Divide	NUM DEN DIRECT ± - DIRECT - + DIRECT + + INDEXED ± - INDEXED - + INDEXED + +	 20.0 20.5 19.75 20.25 20.75 20.0
DMA	Initiate DMA		2.5
DSHL	Double Prec. Left		3.25 + K
DSHR	Double Prec. Right		4.25 + 0.75 K
IMSK	Interrupt Mask		1.75
IOCP	Pulse Out		2.25
JMP	Jump	RELATIVE REL. INDIRECT	1.75 2.25
JSR	Jump to Subroutine	RELATIVE REL. INDIRECT INDIRECT	1.75 2.50 2.25
LD	Load	DIRECT INDEXED RELATIVE REL. INDIRECT	1.5 2.0 2.0 2.5
LI	Load Immediate	IMMEDIATE	1.25
LIM	Limit	RELATIVE	3.5
LOCK	Lock	= 0 ≠ 0	2.75 2.75
MULT	Multiply	DIRECT (MEM < 0) DIRECT (MEM ≥ 0) INDEXED (MEM < 0) INDEXED (MEM ≥ 0)	10.75 10.25 11.00 10.50
OR	Logical OR	DIRECT INDEXED	1.75 2.25
PIN	Parallel Input		2.25
POP	Pop Stack		2.5
POUT	Parallel Output		2.25
PUSH	Push Stack		2.25
RABS	Absolute Value	(+) (-)	2.5 2.7
RADD	Reg. Add		1.5
RAND	Reg. AND		1.75
RCMP	Reg. Compare		2.0

(Table 2 concluded)

Mnemonic	Instruction	Address Mode	Execution Time with a Fast Memory (μs)
RMOV	Reg. Move		1.5
RNEG	Reg. Negate		2.0
RNOT	Reg. Ones Complement		2.0
ROR	Reg. OR		2.0
ROT	Rotate		2.75 + 0.5K
RSUB	Reg. Subtract		1.5
RTI	Return From Interrupt		3.5
RTS	Return From Subroutine		2.75
SHL	Shift Left		2.5 + 0.5K
SHR	Shift Right		2.5 + 0.5K
SHRA	Shift Right Arith		2.75 + 0.5K
SIN	Serial Input		6.5
SKAZ	Skip If AND is Zero	DIRECT INDEXED	2.75 3.25
SKR	Skip If I/O Ready		2.75
SOUT	Serial Output		6.5
ST	Store	DIRECT INDEXED REL. INDIRECT	2.0 2.0 2.25
SUB	Subtract	DIRECT INDEXED	1.5 2.0
Interrupts			
INTERRUPT	Interrupts		3.0
DMA IN	DMA Input Interrupt		2.25
DMA OUT	DMA Output Interrupt		2.25
PWR. FAIL	Power Fail Interrupt		4.5
PWR. UP	Power Up Interrupt		1.25

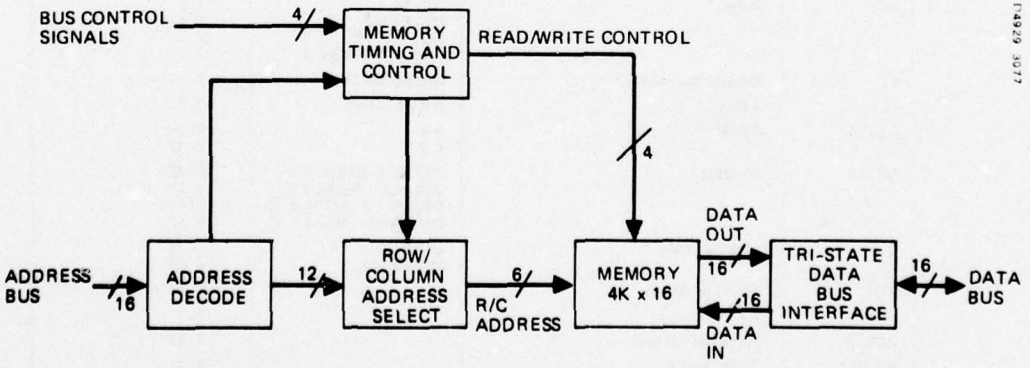


Figure 6. RAM program memory (CM-190).

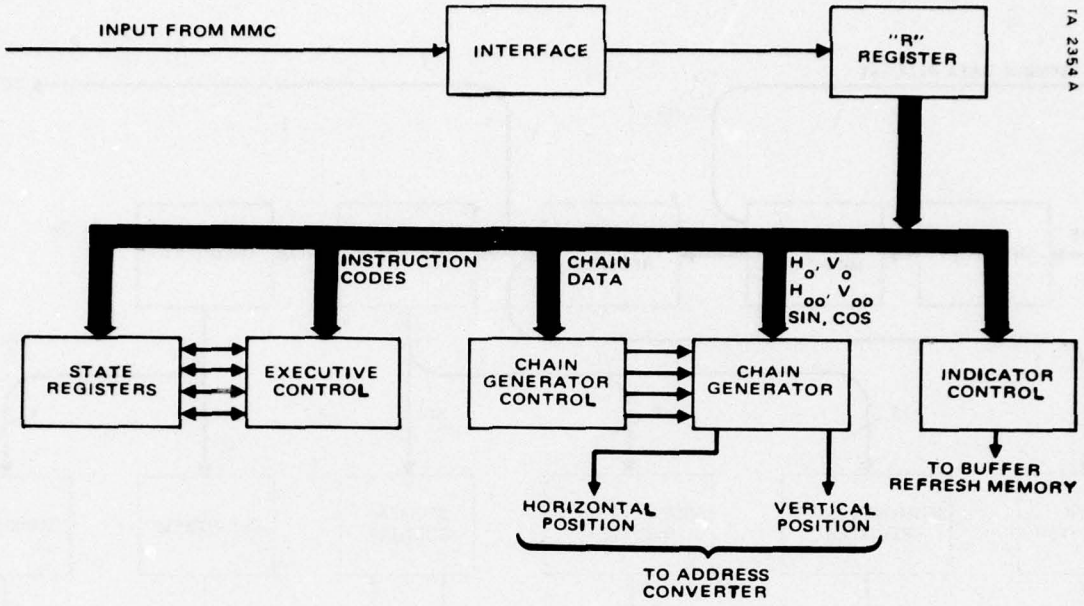


Figure 7. Display generator functional block diagram.

generator is partitioned into four modules: a Symbol Interface Buffer (SI-210); Executive Control (EC-220), and two identical chain generators (CX-250 and CY-260).

Symbol Interface Buffer (SI-210)

The symbol interface buffer module (Figure 8) controls the transfer of data from the display list memory and stores up to sixty-four words in a first in/first out (FIFO) storage register. A data request signal is transmitted to the processor whenever the FIFO is not full. This FIFO interface allows the display symbol generator to operate asynchronously with the microprocessor. The data words received from the display list memory provide complete instructions to the symbol generator for symbol processing. A list of the display generator instructions is given in Table 3. All data is processed through the "R" register and distributed to the appropriate function control registers. Only the required data field is sent to each of the control registers.

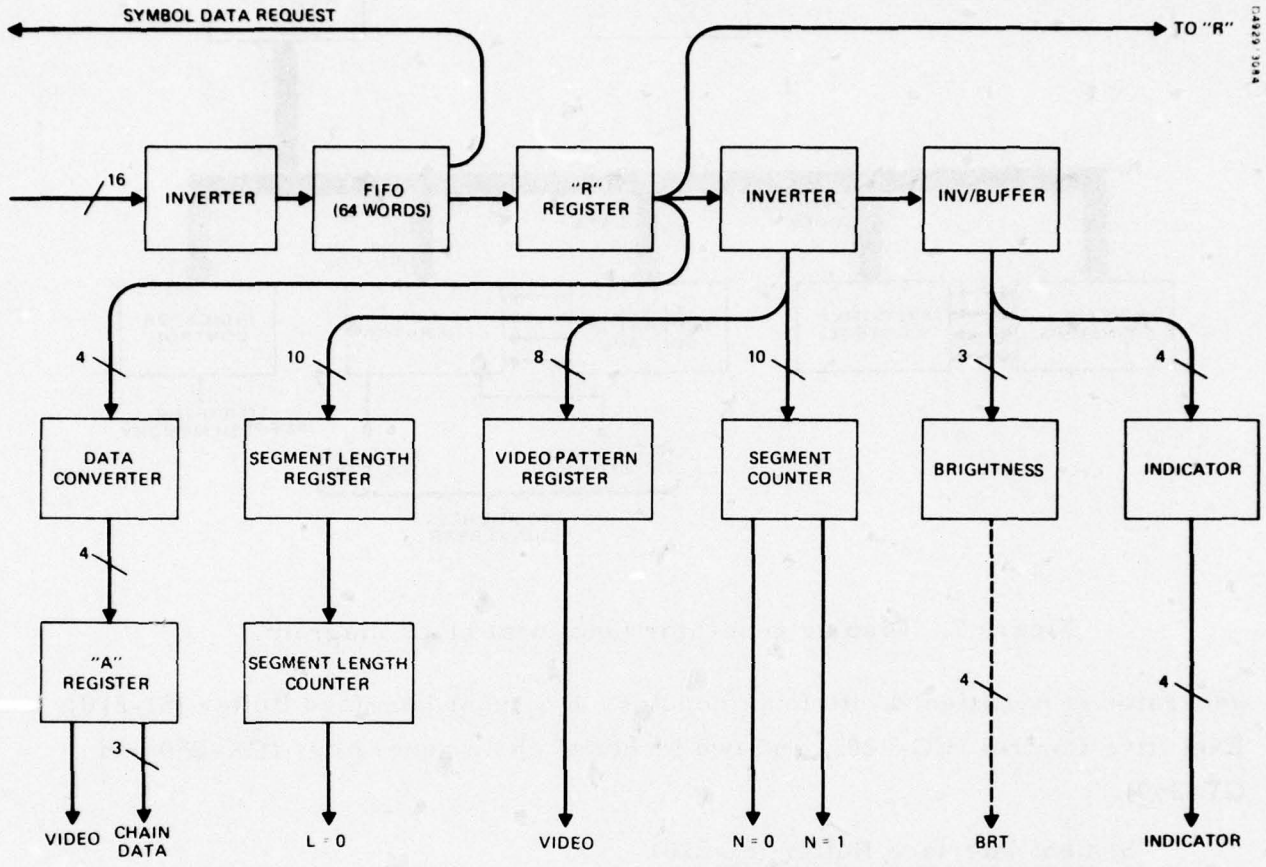


Figure 8. Symbol interface/buffer (S1-210) functional block diagram.

TABLE 3. DISPLAY GENERATOR INSTRUCTION LIST

DATA WORD	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Video Setup																
Indicator	0	0	0	0	0	-	-	-	-	-	-	-	4	3	2	1
Intensity	0	0	0	0	1	-	-	-	-	-	-	CODE		BRT		
Position Setup																
H_{oo}	0	0	0	1	0	H_{oo}										
V_{oo}	0	0	0	1	1	V_{oo}										
H_o	0	0	1	0	0	H_o										
V_o	0	0	1	0	1	V_o										
H_o and Reset	0	0	1	1	0	H_o										
V_o and Reset	0	0	1	1	1	V_o										
Add H_o	0	1	0	0	0	H_o										
Add V_o	0	1	0	0	1	V_o										
Chain Setup																
SIN	0	1	0	1	0	-	$\sin\theta$									
COS	0	1	0	1	1	-	$\cos\theta$									
Video	0	1	1	0	-	-	-	-	Video Pattern							
Length	0	1	1	1	-	-	L-1									
Chain																
Line	1	0	0	0	0	-	N-1 (N = Length of Line)									
Dot	1	0	0	0	1	-	N-1=3 (N = Time on Spot)									
Chain Abs	1	0	0	1	0	-	N-1 (N = No. of Segments)									
Chain Rel	1	0	0	1	1	-	N-1 > 0 (N = No. of 2 BIT Bytes)									
	Chain Data (2 or 4 BIT Bytes)															
No-Operation	1	0	1	0												
	1	0	1	1												
	1	1	0	0												
	1	1	0	1												
	1	1	1	0												
Interface																
Pulse Command	1	1	1	1	0											
List End	1	1	1	1	1											

The data field is the least significant bits of the data words: six bits for segment length, eight bits for video pattern, 10 bits for segment counter, three bits for brightness and four bits for indicator. The "brightness" register is used to control the intensity of symbols in the stroke mode. The "segment length" register stores a ten bit code which defines the length of a line segment that is to be chained to form the required symbology. The segment length is parallel loaded from the segment length register into the segment length counter where it is decremented (counted down) by the clock. When the stroke length has been decremented to zero, a signal is transmitted to the executive module which permits reloading of the segment length into the segment length counter and the process is repeated.

The video pattern register is loaded with an eight bit code which defines a repetitive video pattern that is to be displayed. The data in this register is the instantaneous segment video (on or off). The segment counter is loaded with 10 bits which defines the number of segments in the chain data. The contents of this register is decremented by one as each segment is utilized, thereby keeping track of the number of remaining segments. When the number of remaining segments (N) equals 1, a signal is transmitted to the executive module and the chain is terminated.

Chain data is sent from the "R" register through the data converter which converts relative data to absolute data format required by the chain generator modules. After conversion, the data is stored in the "A" register and transmitted out to the chain generator as required. The data converter operates on the chain segment "next to be displayed."

Executive Control (EC-220)

This module (Figure 9) performs executive control of three symbol generator modules, the SI-210, CX-250, and CY-260 by defining the operations to be performed at each clock step. The instruction code and segment counter status received from the symbol interface buffer module (SI-210) and the executive state register are all presented to the Instruction Decoder. The decoder interprets the inputs to define 63 operational states which are a mix of single instruction, internal control, and chain subroutine functions. These operational states are presented as an address code to the Function Coder. The function Coder creates control signals for each of the functional blocks

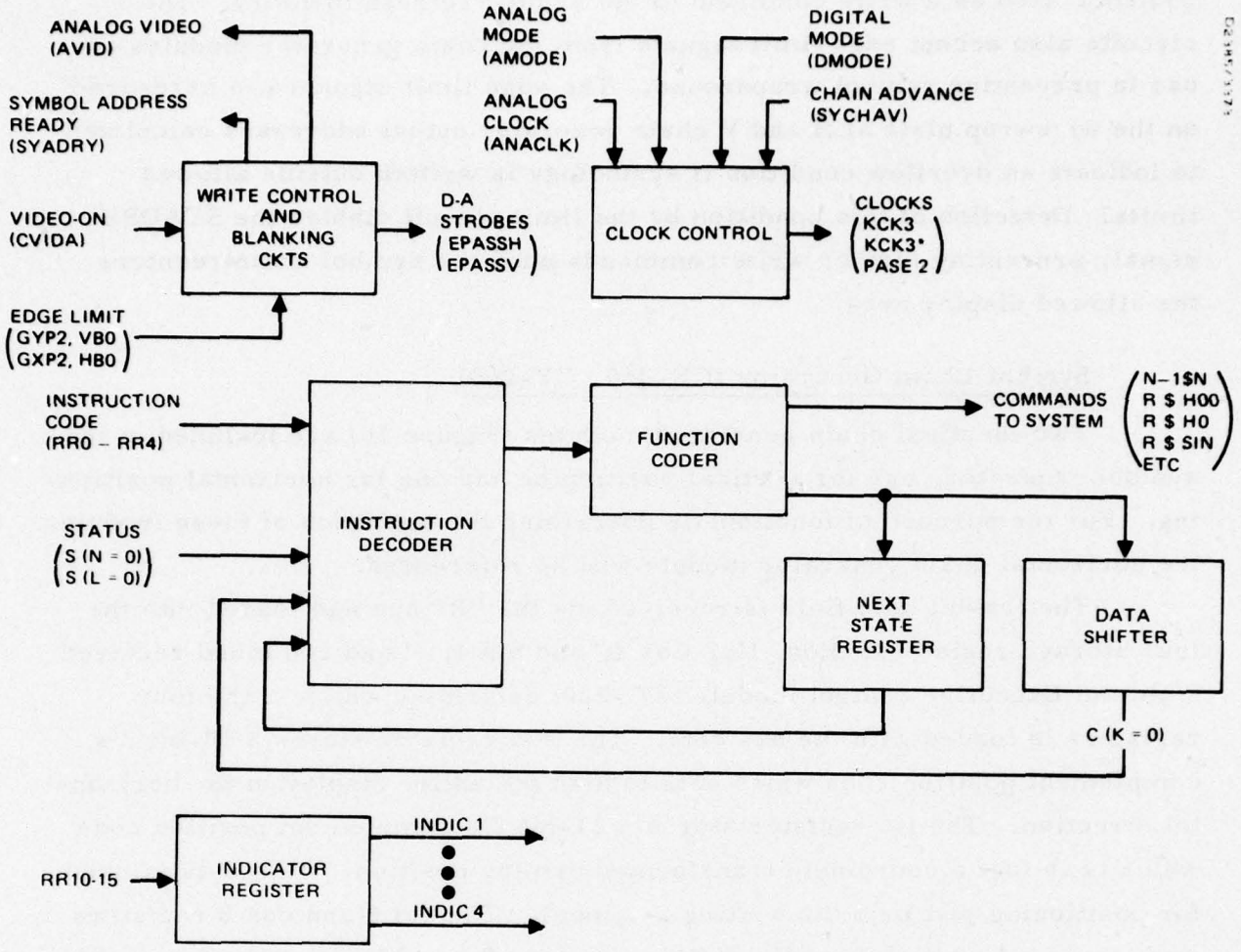


Figure 9. Executive control (EC-220) function block diagram.

and registers comprising the symbol generator. Next state and chain subroutine jump address feedback is provided via the Next State Register. The Data Shifter function acts to control access to chain direction data packed in chain data words. The Clock Control acts to create gated clocks when commanded by the analog clock or chain advance requests. The selection of the two basic symbol generator modes, calligraphic or in-raster, are commanded by the AMODE or DMODE commands and select which of the two clock commands to use. The modular scan converter is hard wired by jumpers in the wire wrap baseplate to always be in the digital mode. The Write Control and Blanking circuits accept a symbol video signal input CVIDA and create an analog (calligraphic) blank-unblank signal and a symbol address ready

SYADRY used as a write command to the symbol refresh memory. The circuits also accept edge limit signals from the chain generator modules for use in preventing symbol wraparound. The edge limit signals are hardwired on the wirewrap plate at H and V chain generator output addresses calculated to indicate an overflow condition if symbology is written outside allowed limits. Detection of this condition by the limit circuit diables the SYADRY signal, preventing further write commands until the symbol chain reenters the allowed display area.

Symbol Chain Generator (CX-250, CY-260)

Two identical chain generator modules (Figure 10) are included in the symbol generator, one for vertical positioning and one for horizontal positioning. For the purpose of functionally describing the operation of these modules the horizontal chain generator module will be referenced.

The ten-bit data field is received via the "R" bus and loaded into the four storage registers: Hoo, Ho, Cos θ, and Sin θ. Load command received from the Executive control module (EC-220) determine which of the four registers is loaded with the bus data. The Hoo register stores a 10-bit 2's complement position code which acts to bias the entire display in the horizontal direction. The Ho register stores a 11-bit 2's complement position code which is in fact a coordinate transformed display position. This data is used for positioning just prior to writing a symbol. The sin θ and cos θ registers each store a 10-bit code which defines an angle θ by which a chain is rotated.

To generate a chain (or straight line segment) a "0" or "1" is added to or subtracted from each X and Y accumulator at successive clock times. A line can therefore be drawn in any one of eight directions, using a three-bit code, as shown in Figure 11. A fourth bit would determine whether or not the video is on.

To rotate a chain by an angle θ, a coordinate transformation is performed. This transformation has the form:

$$X_i' = X_i \cos \theta - Y_i \sin \theta$$

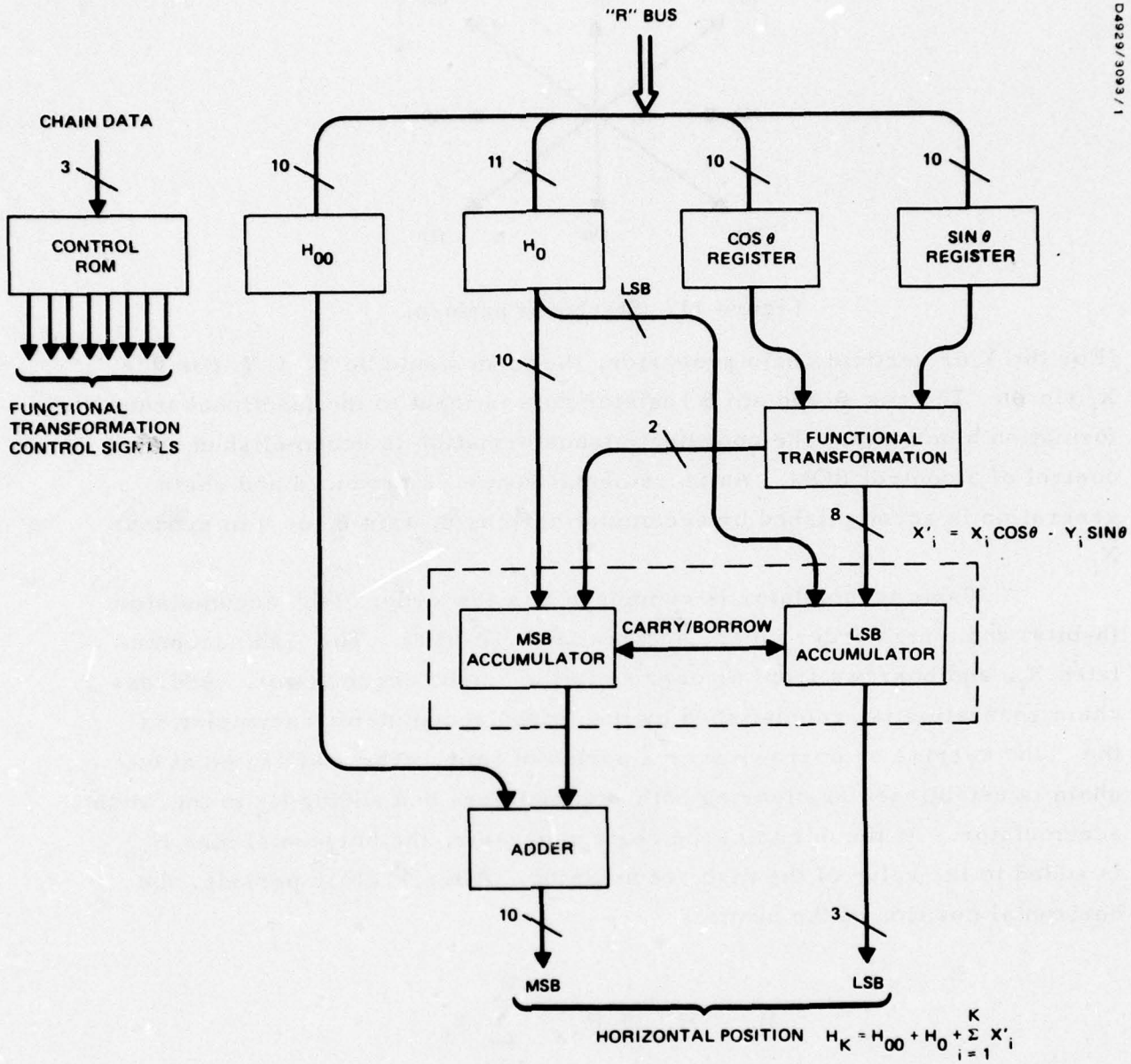


Figure 10. Chain generator (CX-250, CY-260) functional block diagram.

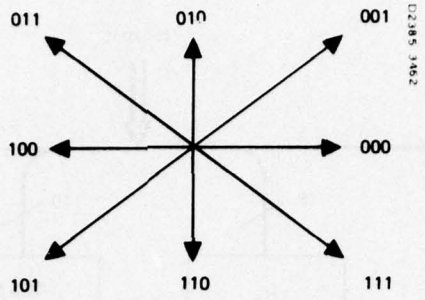


Figure 11. Starburst pattern.

(For the Y or vertical chain generator, the form would be $Y_i' = Y_i \cos \theta + X_i \sin \theta$). The cos θ' and sin θ register data is input to the functional transformation block where the coordinate transformation is accomplished under control of a control ROM. An incremental vector is produced and chain generation is accomplished by accumulating $\pm\cos \theta$, $\pm\sin \theta$, or 0 to produce X_i.

A 20-bit accumulator is composed of a low order "lsb" accumulator (8-bits) and a high order "msb" accumulator (12-bits). The "lsb" accumulates X_i', and borrows from or carries to the "msb" accumulator. Address chain generation is accomplished by the "msb" accumulator accumulating the "lsb" carries or borrows over a period of time. The starting point of a chain is established by clearing both accumulators and adding H_o to the "msb" accumulator. At the output of the chain generator, the horizontal bias H_{oo} is added to the value of the msb accumulator. After k clock periods, the horizontal position of the beam is

$$H_k = H_{oo} + H_o + \sum_{i=1}^{k} X_i'$$

Similarly

$$V_k = V_{oo} + V_o + \sum_{i=1}^{k} Y_i'$$

The 10-bit address data field of the "msb" accumulator and the three most significant bits of the "lsb" accumulator are made available at the module connector. The symbol refresh memory addresses use only the "msb" address field and the highest ordered bit of the "lsb" address field.

The control ROM receives chain data, three bits at a time from the "A" register located on the Symbol Interface Buffer module (SI-210) and provides signal outputs that control the chain generators. After each segment is drawn, the chain data on the interface buffer module is shifted four places to the left, inputted to the "A" register where the video bit is stripped away and the resulting next three bits of chain data are sent to the control ROM.

Refresh Memory Timing and Control

The output of the symbol generator is a digital output suitable for use on a calagraphic display. All that is required is the addition of a suitable D/A converter, which has in fact been provided as part of the HRVSD program. This permits the presentation of symbolic information on a Head-Up or other stroke Display. Since the primary function of the symbol generator is to provide the pilot with a vertical situation display (VSD) in a TV format, the output of the symbol generator must be sent to a field refresh memory for reformatting. This field refresh memory and its associated input and output reformatting was the subject of the Phase III study effort, and the resulting hardware was incorporated into the complete system delivered at the end of the current effort (Phase IV). For the sake of continuity and completeness, a brief overview of the display requirements, refresh memory configuration and timing is presented here. A more complete description is the Phase III report, ref. 3.

Display Requirements Overview

The field refresh memory functions as the interface between the display generator and the CRT display. As such it must provide the required symbology in a format compatible with both 875 and 525 line TV. The resultant display is a composite presentation of flight data symbology superimposed over sensor video.

The flight data display and display data arrangement for the pilot's VSD is shown in Figures 12 and 13. The entire 7.5 x 10 inch CRT display

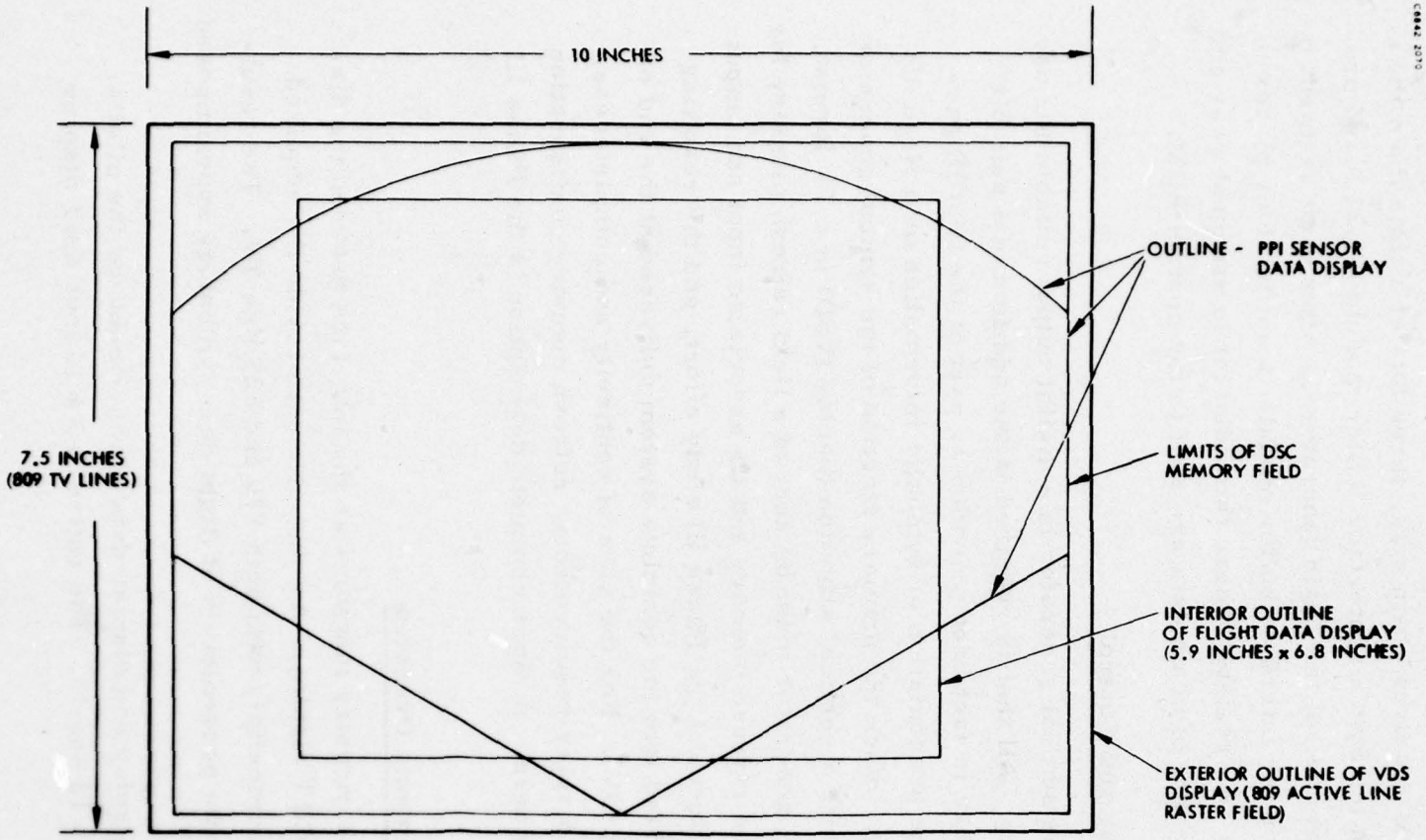


Figure 12. Display data arrangement-pilots VDS.

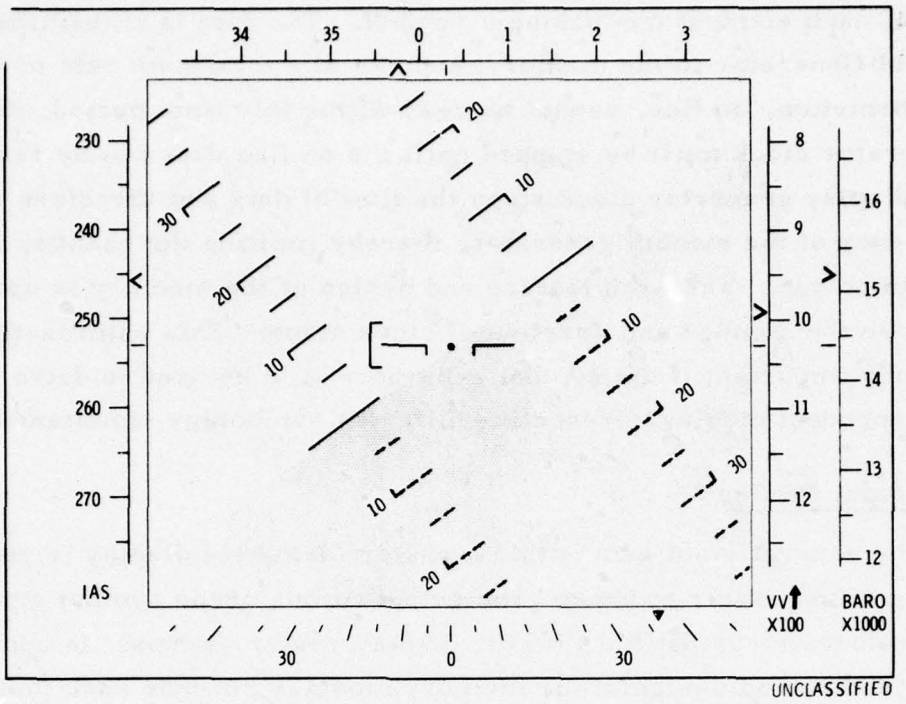


Figure 13. Flight data display.

area is available for display of data. The central area of the VSD is used to display the pitch ladder, attitude reference data and angle of attack symbology superimposed over sensor video. In addition, sky/ground shading is provided as a pilot orientation aid. The outline of the PPI sensor data display is also indicated in Figure 12. Note that the sensor video is confined to the central area permitting an easy to read presentation of flight data. The presentation of the pitch group is also confined to the central area. Therefore, the only symbology that must rotate in-raster is contained in the central area.

By inspection of Figure 12, the border area allocated for flight data display can accommodate vertical and horizontal tapes displays of up to 6 inches in length. As developed in the Phase I report, ref. 2, heading and roll angle data scales are placed at the top and bottom border areas of the display. An airspeed tape, either in knots or mach number, is placed on the left edge of the display. Aircraft altitude and vertical velocity tapes are located at the right side of the display.

Input Timing

The input to the field refresh memory (output of the Symbol Generator) consists of the X and Y (up to 12 bits are available if required) address or

position of each element composing a symbol. The data is transmitted from the Symbol Generator to the memory modules at a maximum rate of 4 MHz. If the information, on line, cannot be read within this time period, the display generator clock must be stopped until the on line data can be read. Stopping the display generator clock stops the flow of data and therefore affects the efficiency of the symbol generator, thereby limiting the quantity of displayed symbology. The architecture and design of the memory is optimized to minimize the number and duration of clock stops. This optimization is particularly important if the symbol generator is to be used to drive two or more independent displays presenting different symbology simultaneously.

Output Timing

The generation of data within a raster formatted display is governed by the timing of the raster sweeps. The output timing of the symbol generator must therefore be compatible with the display raster sweeps. In addition, the architecture and design of the memory modules must be such that the resulting output timing does not "tie up" the memory, during readout, for an appreciable time. When the memory is being readout for display, data cannot be read in and hence a clock stop signal must be generated which, in turn, reduces the efficiency of the symbol generator as described in the previous paragraph.

To generate a "dot" at a given point in the display field, it is necessary to unblank the CRT beam the instant it traverses a given point in the raster gridded field. Figures 14 and 15 reflect the output timing requirements for both the 875 and 525 line modes.

Refresh Memory Functional Design

A functional block diagram of the refresh memory modules and its associated input and output format logic required to provide the required timing and in-raster presentation of video is shown in Figure 16.

The major elemental blocks shown consist of the input format logic, memory modules, output format logic and the post processor. The heart of the system is the memory modules which function as intermediate storage of digital symbolic data to permit the reformatting of incoming data to a format compatible with standard television. The input format logic is the interface between the display generator and the memory. The input symbolic digital

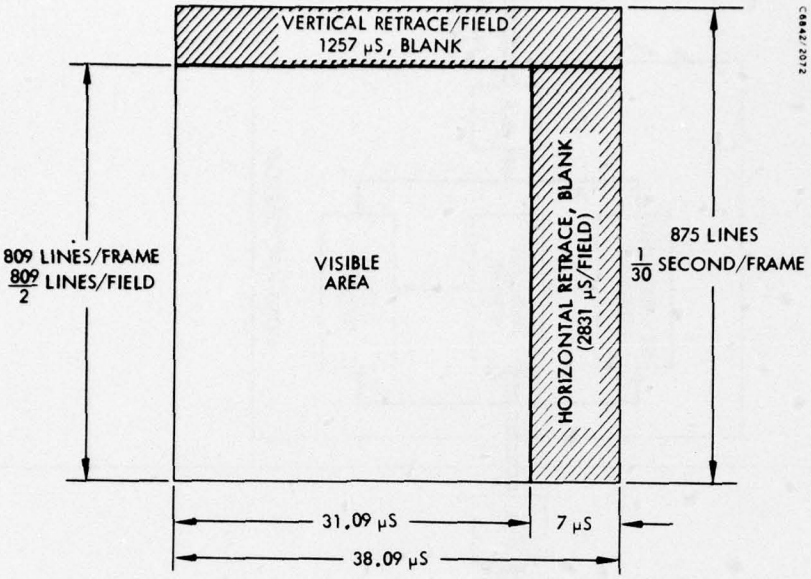


Figure 14. 875 line TV timing diagram.

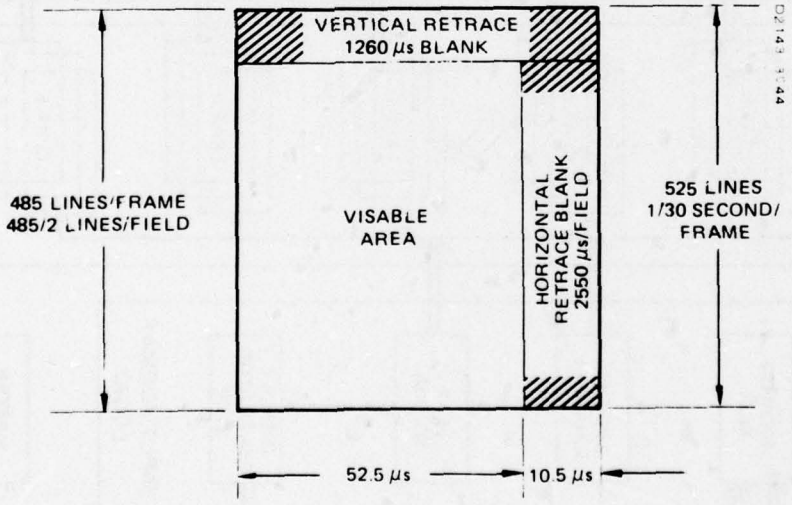


Figure 15. 525 line TV timing diagram.

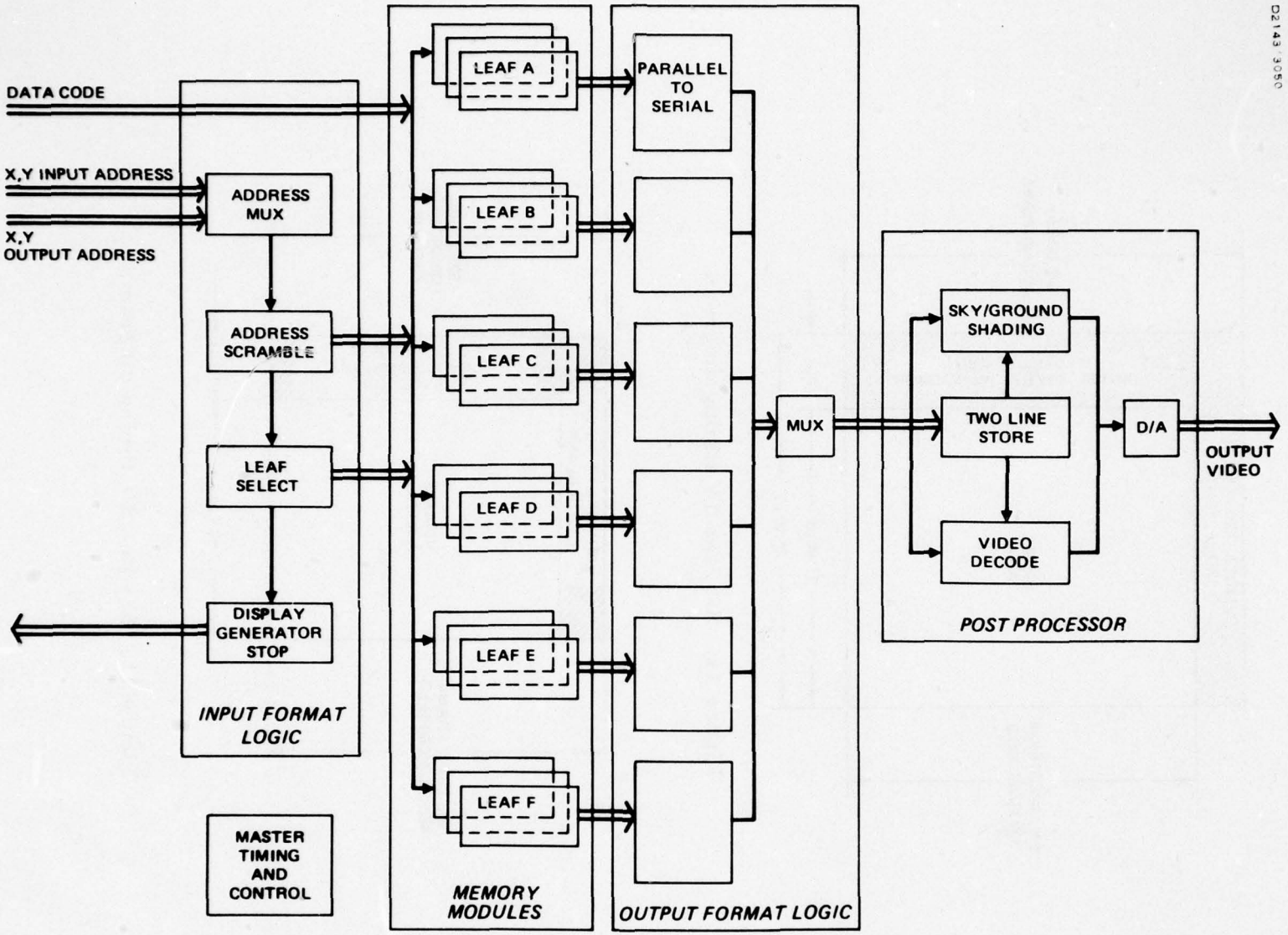


Figure 16. In-raster memory modules functional block diagram.

data is received from the display generator and the correct memory element is selected, for storage of data. The output format logic access the memory just prior to and in synchronism with the television raster. The post processor element processes the TV compatible serial data for image enhancement to provide a high quality presentation.

Input Format Logic

The input format logic receives the data code to be stored and its associated X, Y display address from the display generator. In addition, the X, Y address of data to be read out of memory is received from the master timing and control module. The data code is a 3 bit parallel "pattern code" which defines the intensity distribution of the particular data bit stored for display. The data code is sent directly to the memory via the input format logic. In synchronism with the data code, the address or position of the data code referenced to the display is received as a 9 bit X and 9 bit Y (1 part in 512) parallel signal. The address multiplexer selects the X, Y input address during the memory write portion of the cycle and routes this data address to the address scrambler.

The address scramble function is two fold. First it selects the particular leaf in memory (1 of 6) for storage of the incoming data, and second it selects a particular memory cell according to the memory architecture shown in Figure 10. The address scrambler is a high speed binary divider which divides the 9 bit X address by 6 and the 9 bit Y address by 3. The remainder of the two divisions are combined arithmetically and the resultant signal is utilized to select 1 of 6 memory leaves.

Memory Modules

The entire memory consisting of 384 x 512 x 3 bits is contained on 18 memory modules. The memory is divided into six leafs. Each leaf consists of three 4K x 8 bit memory modules. Each leaf is three deep to provide storage of the 3 bit data code. To execute a readout cycle, all six leafs are addressed by the same X_M, Y_M address simultaneously and eight 3 bit bytes, for a total of 48 per leaf is outputed in parallel to the output format logic. 3 bit bytes for the 6 memory leafs, are outputed in parallel from the memory. These 48 3-bit bytes must be clocked to the display serially for presentation in-raster.

Output Format Logic

The output format logic consists of six sets of 8 bit parallel to serial converters, one converter set per leaf. During the read cycle eight bits per leaf or a total of 48 bits (X3 for intensity coding) are clocked out of memory in parallel and stored in the parallel to serial converters. These 48 bits are then "unscrambled" and clocked out serially at a 16 Megahertz (MHz) rate. The 16 MHz rate corresponds to the 875 line display mode line rate. In the 525 line mode the data is clocked out at approximately 6 MHz. Each element of display data, consisting of a 3 bit code is outputed to the post processor for conversion to analog video.

Post Processor

The post processor functional element provides the required signal conditioning and interface between the symbol generator and display. It performs four primary functions as follows:

1. Video decoding
2. Sky/ground plane shading
3. Edge blanking
4. Digital to analog video conversion.

Programmer's Panel

The Programmer's Panel is an Intellec MDS 800 microprocessor development system used as an interface controller for the MMC (AN/yuk-30) microcomputer. The purchased unit includes the following plug in modules:

- Front Panel
- CPU
- DMA

Additional spare card slots are provided in the MDS chassis for future system I/O modules. A functional block diagram of the MDS is shown in Figure 17.

To provide communications between the MDS and the MMC, a special interface module was developed and is housed in the MDS chassis. Also part of the Programmer's Panel function is a visual readout of the operation of

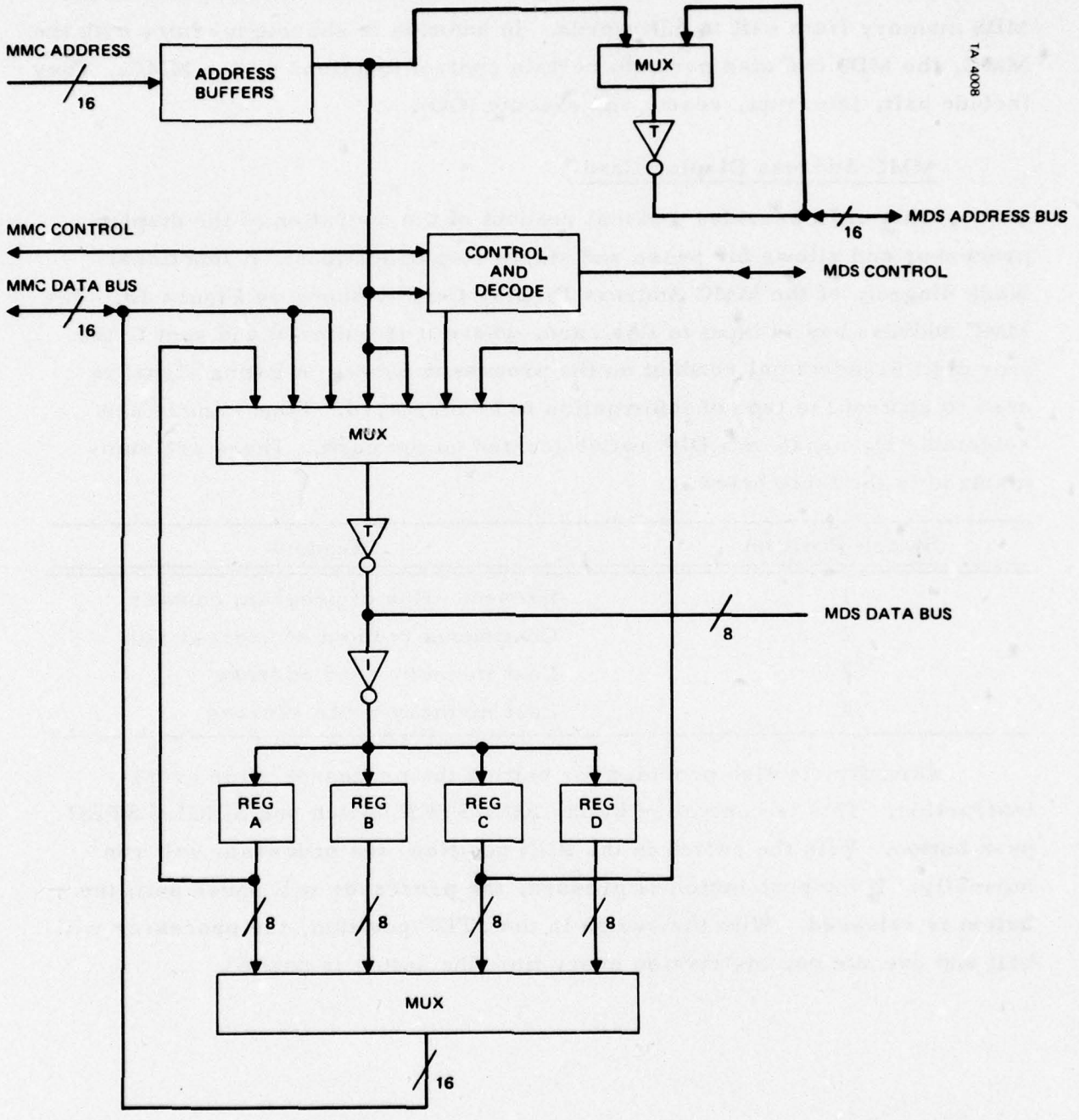


Figure 17. MMC-MDS functional block diagram.

the display processor which is provided for by the MMC Address Display module.

All MDS memory is shared with the MMC. Since the MDS is an 8 bit processor and the MMC is a 16 bit processor, two MDS words are combined and treated as one word by the MMC. This reduces the effective size of the MDS memory from 64K to 32K words. In addition to sharing memory with the MMC, the MDS can also perform certain control functions on the MMC. They include halt, interrupt, reset, and execute (GO).

MMC Address Display Card

This card provides a visual readout of the operation of the display processor and allows for pause and single step operations. A functional block diagram of the MMC Address Display Card is shown in Figure 18. The MMC address bus is input to this card, where it is buffered and sent to the four digit hexadecimal readout on the processor panel. A gating signal is used to control the type of information to be displayed. Four signals are selectable by means of a DIP switch located on the card. These are summarized in the table below.

Switch Position	Readout
1	Present value of program counter
2	Continuous readout of address bus
3	Last memory read address
4	Last memory write address

Circuitry is also provided for halting the processor after every instruction. This is controlled by the RUN/STEP switch and SINGLE STEP push button. With the switch in the RUN position, the processor will run normally. If the push button is pressed, the processor will pause until the button is released. With the switch in the STEP position, the processor will halt and execute one instruction every time the button is pushed.

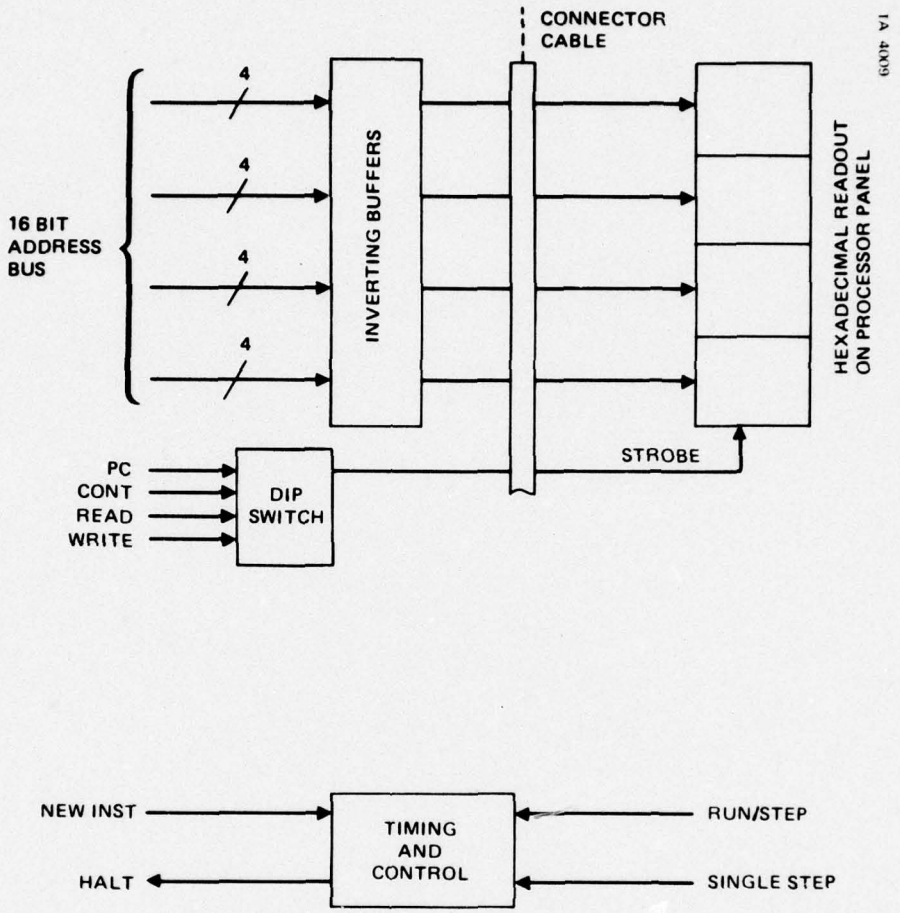


Figure 18. MMC address display – block diagram.

SECTION 3
THE APPLICATION OF COLOR TO THE HIGHLY RELIABLE VDS

INTRODUCTION

Color is a characteristic of our visual world that is becoming increasingly important as a means of transferring information between machine and man. The importance of color has been underscored by the increasingly stringent demands being made on modern aircraft performance and the incorporation of increasingly sophisticated weapon systems. Color display such as electromechanical flags, pointers, annunciation, lights and optical projection devices, have been used in modern aircraft. Serious interest in the use of color for airborne information displays has been relatively recent. This interest has been brought about in part by the trend toward integrated display presentations for the pilot with a multiplicity of information presented on a single display surface. Color coding of information enables the displayed information density to be increased and the assimilation time to be decreased. Studies have also shown that color coding is the preferred method of alerting the pilot to a critical situation.

The single item that has prevented wider use of color for presentation of information in the cockpit has been the display device itself. Giving due recognition to the need for a high brightness, high resolution color display for use in a tactical aircraft, NADC awarded a contract to Hughes Aircraft Company (Contract N62269-70-C-0381 with Mr. W.G. Mulley of NADC acting as Project Engineer), ref. 4. Although the study effort was directed toward a map display application, most of the display technology effort is equally applicable to a Vertical Situation Display.

The approach taken in the current effort, "The Application of Color to the VDS," is to update the comprehensive survey of the color display technology survey conducted during the above mentioned contract. An effort was

4. R.N. Winner, M.N. Ernstoff. A Color Television Monitor for the Display of Standard Aeronautical Charts in Advanced Aircraft – A Design Study, Hughes Aircraft Co., HAC Ref. No. C0381, 3/71.

made to concentrate in only those areas which offered the most promise. Also included is a discussion of utility of color for both video presentations and symbolic presentations.

VIDEO DISPLAYS

The use of color in pictorial or sensor displays is largely unexplored; although, some likely applications relevent to the VDS can be postulated. For instance, when color is applied to sensor video, it may be used to encode low contrast imagery. In this case, adding a dimension of discernibility, i.e., chromaticity, to targets that previously contained little or no difference in brightness between themselves and their background. The potential is to provide greater recognition ranges than with monochromatic displays. An extreme example would be a target having zero brightness difference with respect to its background. This could occur, for instance, when an E/O sensor images an olive-drab vehicle against a light-brown desert background, under sun angles that are aligned along the weapon line-of-sight. For a monochrome display under this condition, picture contrast (target-to-background) would be near zero, but with color added very high chromaticness differences can be obtained, especially if the operator enhances the display by increasing chroma gain.

This is the same effect that was no dramatically illustrated to early workers in television when color was first applied to remote telecasts of sporting events. There, under cloudy skies and with the somewhat insensitive image pickups of the time, it was scarcely possible to distinguish one team from another on the monochrome monitor. With color, the veil of confusion was lifted. The formerly gray and muddied jerseys took on a new meaning in color identifying the green team vs the gold team; it was even possible to see who had the ball!

The foregoing example is relevant to military displays because much of the sensor imagery of interest is often received in the aircraft under adverse conditions contributing to low contrast and high background noise.

Conversely, color has been shown to have little value in improving acquisition performance in situations where high-contrast medium resolution imagery is used. The point here is that if the image contrast is good enough to begin with, color is not going to enhance it.

Unfortunately, color studies have tended to look at narrow aspects of the problem, usually because of equipment constraints, and although their

conclusions are correct for the narrow aspect under study, the conclusions cannot be applied to the generalized airborne display requirement.

One application where color is believed to be important is in the display of video from high-resolution, IR sensor systems. Here, the potential application is in extending the dynamic range of the display to accommodate sensor video containing meaningful amplitude differences over a range that exceeds the perceptible dynamic range (8 to 10 shades of gray) obtainable with monochrome displays. By artificially encoding specified amplitude regions with a predetermined scale of hues, it becomes possible to discriminate targets on the basis of temperature from their background in a manner analogous to that followed with so-called false-color IR films. Hughes constructed such a display for use with an advanced forward-looking IR (FLIR) system, designated MAFLIR. The results obtained in system trials where inconclusive, however, due to the limitations inherent in the system and in the penetration phosphor CRT's that were available at that time. In addition, early high-resolution FLIR systems had unfavorable duty cycles which resulted in a significant loss in brightness in any real-time display of their output. Also, the penetration technique employed at that time utilized a barrier layer and phosphors which operated at lower energies and hence lower brightness than contemporary components using this technique. The combination proved to be too dim for the airborne environment, requiring nearly total darkness for the operator to discern hue differences. Nevertheless, its implementation proved, within controlled-ambient laboratory conditions, that the two-primary, color penetration technique was capable of producing at least four discernible hues in high-resolution (excess of 800 TV limiting lines).

SYMBOLIC DISPLAYS

Contemporary geometric and alphanumeric coding systems have reached a level of display complexity that tax man's ability to process the information with the degree of comprehension that is required by the mission. While there is no evidence that the information presented on the AIMIS VDS is approaching a condition of near saturation, the question of whether or not the addition of color will improve or degrade pilot performance is a valid one. A number of past studies that were reviewed provided solid evidence for the use of particular types of color coding for specific tasks on particular types of display under a given set of conditions. However these studies, in general, have not dealty with color CRT's.

The following excerpts from the Semple et al (1971) study present a brief summary of the data found in studies examining the utility of color coding for specific tasks under different viewing conditions for non-CRT displays.

Advantage of Color Coding

1. Color codes are best for the location of targets or for gaining attention devices. Color coding is less effective than other coding methods for identification tasks.
2. Performance is improved; i.e., search times and identification errors are reduced when color coding is used in conjunction with alphanumeric or geometric codes, ref. 5.
3. Color coding provides an additional dimension for the presentation of information.
4. Color codes used in conjunction with other codes or symbols can increase the amount of stimulus information presented in a given message from 9.51 to approximately 25.36 bits, ref. 5.
5. The sensation of color is common to all color-normal observers and therefore requires little additional training.
6. Color brightness as well as color hue is effective for coding, ref. 6.
7. Color is excellent for coding states or status in visual displays.
8. Some evidence suggests that color enhances performance in certain interpretation, reading and "Higher Cognitive" tasks, ref. 7.
9. Color codes facilitate counting tasks on complex displays, provided the color of the target is known in advance and only a few colors are used.
10. Relearning and transfer of training appear to be enhanced with the use of color.

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5. Anderson, N.S. and Pitts, P.M. "Amount of Information Gained During Brief Exposures of Numerals and Colors." Journal of Experimental Psychology, Volume 56, Number 4, Pages 367-369, 1958.
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Disadvantages of Color Coding

1. The average color-normal person can discriminate only about nine hues of surface color on an absolute basis under ideal conditions, and even fewer under adverse conditions. (Only four hues on CRT generated displays.) Ref. 8.
2. Some people are color-defective; about 8 percent of all males and 0.4 percent of all females.
3. Color discrimination is seriously degraded when surface colors are viewed under highly chromatic light sources.
4. Signals or color patches of small dimensions, 20 minutes or less in visual angle, cause normal subjects to show certain characteristics of anomalous color vision. Color codes recommended for two degrees or larger do not apply to 20 minutes or smaller sources of light.
5. Numeric codes (followed by geometric codes) are best for identifying, counting, verifying, and comparing tasks, ref. 9.
6. The use of non-relevant, unusual or culturally contradictory colors tend to complicate visual search tasks, ref. 10.

Most applied research pertaining to colored displays has been concerned with the presentation of symbolic information. Although some investigations have found negative results, the majority of experiments have proven that the application of color as a coding dimension enhances performance in visual search tasks with symbolic displays (alphanumerics and shape coding). The added dimensionality of color also increases the information rate that can be presented in a given display.

A significant factor is the fact that none of the studies examined addressed the problem of color coding on colored CRT displays. The effect of electronic display phosphors (for colored displays) under changing illumination conditions may produce significantly different results. An in depth examination of this effect, although beyond the scope of this present effort appears warranted.

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8. Conover, D. W. and Kraft, C. L. The Use of Color in Coding Displays. WADC Technical Report 55-471 (AD 204 214), Aero Medical Laboratory, Wright Air Development Center, Wright-Patterson Air Force Base, Ohio, October 1958.
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VDS DISPLAY PERFORMANCE REQUIREMENTS

The performance requirements for the Highly Reliable VDS were initially developed during Phase I, ref. 1. An operational requirement analysis was first conducted which took into account the crew, display subset, the AIMIS aircraft missions and sensor complement. In summary, the operational requirements analysis showed the need for three basic functional capabilities. These included, 1) a display of symbology for flight director capability, 2) a TV presentation of electro-optical sensor data and 3) a display of radar sensor data.

The purpose of the performance requirements analysis was to convert the general operational requirements to specific mechanization requirements. A summary of the performance and mechanization requirements for the CRT indicator is given in Table 4. The suitability of a color CRT for use in the Highly Reliable VDS can therefore be determined by comparing its performance capability relative to the established CRT requirements given in Table 4. Mechanization tradeoffs conducted during the Phase I effort indicated the need for a resonant deflection system for generation of the TV raster for a CRT display if the power and reliability requirements were to be met. In addition, the alphnumeric symbology must be presented in-raster for a typical flight data display, Figure 3a. This is so because of deflection power requirements, reliability, available writing time and brightness considerations.

TABLE 4. VDS DISPLAY INDICATOR PERFORMANCE AND MECHANIZATION REQUIREMENTS

Size:	7.5 x 10 inch useable (12 inch diagonal CRT)
Brightness and Contrast:	Sufficient to provide eight shades of gray at 10,000 ft-candle ambient illumination (1200 ft-lamberts with efficient contrast enhancement
Resolution:	800 lines vertical, 1000 lines horizontal
Display Format:	875 line TV, 30 Hz frame rate 525 line TV, 30 Hz frame rate
Writing Speed:	322,000 inches per second max (for a 7.5 x 10 inch CRT in the 875 line mode)
Power:	100 watts
Reliability:	4000 hours
Displayed Information:	Radar Video EO Video Symbolic Data

COLOR DISPLAY ALTERNATIVES

During conduct of Navy Contract N62269-70-C-0381, ref. 4, a comprehensive survey of display components suitable for use as a color display was accomplished. The chief difference in requirements between a map display and a VDS application is related to the required visibility. A two primary color scheme, although found to be attractive from the standpoint of simplicity, was ruled out for use in the map display application as not being capable of displaying essential color map information with sufficient color saturation to provide the required visibility. The color display generation alternatives reviewed can be categorized into four groups as follows: 1) element sequential systems, 2) optically combined systems, 3) field sequential systems and 4) other techniques. A complete tabulation of all techniques reviewed during the earlier study, ref. 4, is given below.

Element Sequential Systems

- Shadow Mask CRT
- Trinitron CRT
- Light Valves

Optically Combined Systems

- Trinescope
- Rear Projection Screen
- Field Lens

Field Sequential

- Electromechanical Filters
- Liquid Crystal Filters
- Ceramic Filters

Other Techniques

- Beam Penetration CRT – Voltage Sensitive
- Beam Penetration CRT – Current Sensitive
- Direct View Color Storage Tubes

- Chromatron
- Two-Color Thin Tube
- Banana Tube
- Apple and Goodman Tubes
- Sunstein Systems

The underlined items represent the technology that offered the most promise for application to color television map displays. For the VDS application, the beam penetration CRTs should be included in the list.

For the present contract, only those color display approaches which appear attractive for the VDS application and which some effort has been expended by industry to gain improved performance, have been reviewed. In addition, any new technology which has shown promise for use as a color display has been reviewed.

In the new technology category, the liquid crystal matrix display current under development by Hughes Aircraft Company has been reviewed.

Elemental Sequential Systems

The three elemental sequential systems include the Shadow Mask CRT, Trinitron CRT and the Light Valves. Of these three devices, only the Trinitron or "Trinitron Type" CRT has both attracted industry attention over the past five years and appears to have further potential for improved performance for a VDS application in a two-color system. The light valve system was not considered because of its inherent limitation of brightness and resolution.

Trinitron CRT

The Trinitron color CRT was developed by Sony Corporation of Japan, to improve the color picture tube by reducing its complexity. Its two unique features are the Single Gun Structure and the Aperture Grille. During the past two years, several other corporations have developed very similar color CRTS, i.e., Lynatron by Sharp Corp. Due to the superior performance and reduced complexity, the color televisions produced for home entertainment are incorporating this type of CRT rather than the shadow mask CRT. It would not be surprising to see the shadow mask CRT completely phased out and replaced by the single gun aperture grille CRTs within the next two years.

The single gun structure of the Trinitron CRT is illustrated in Figure 19. This structure produces the three electron beams within a neck length that is very short compared to other multi-beam guns. A system of first and second beam deflectors located near the tip of the gun cause proper convergence of the beams into a common spot at the aperture grille. The operation is as follows. Electrons emitted from the cathode pass through their respective control grids, the RGB apertures, and thence are commonly converged by the electrostatic electron lens field at A. The beams then converge at the center of the main electron lens B, which forms a common focus field. This focusing method accounts for the low coma and astigmatism of the TRINITRON design. Upon exiting the field at B, the beams diverge and enter a system of first and second beam deflector plates which are interposed between the tip of the gun and the viewing screen.

The green beam has been chosen to be on axis in this system since it accounts for most of the information in the color scene, i.e., green is 59 percent of the content in the NTSC system of color primaries and it is also the wavelength to which the eye is both the most responsive and has the

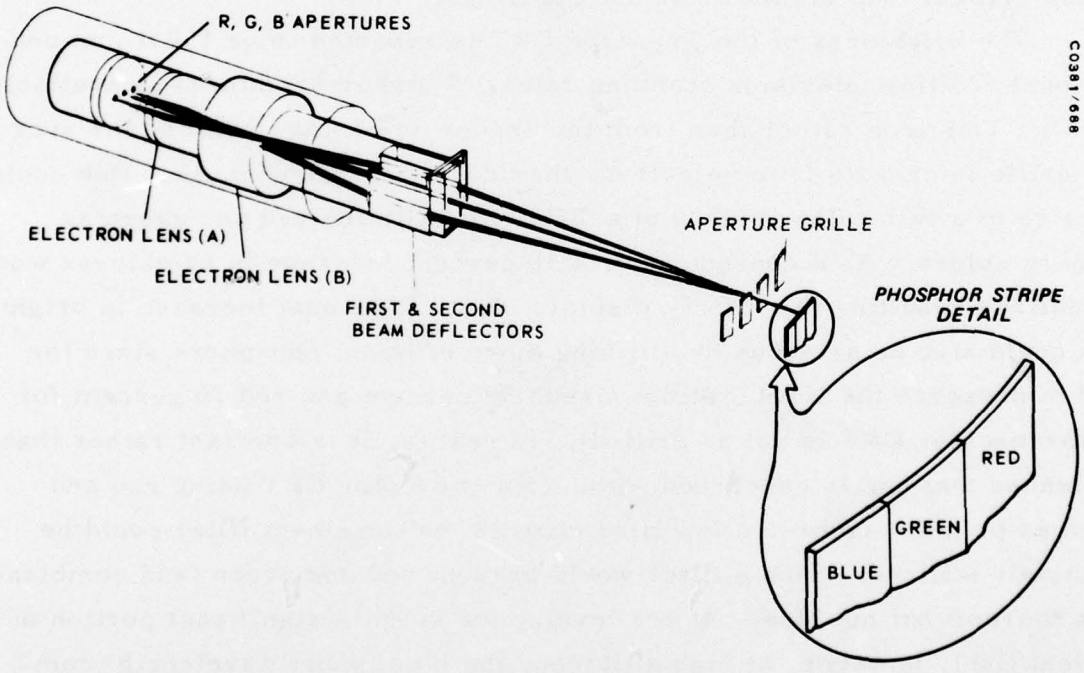

Figure 19. TRINITRON CRT.

greatest resolving power. Accordingly, it is the sharpest in this case because it passes undeviated through the converging lens, focusing lens, and beam deflectors. The red and blue beams can be slightly deteriorated, however, without seriously degrading the resolution. The outstanding performance of the TRINITRON is due in part to this judicious assignment of beams and also to the fact that the convergence has been reduced from a multi-dimensional problem as in the shadow-mask CRT, to essentially a single-dimension (the horizontal plane).

The simplicity afforded by this approach means that the electron gun is producible using standard production techniques and also is capable of higher tolerance to shock and vibration. The remainder of the tube design would be expected to be as susceptible to the airborne vibration and magnetic field environment as the shadow mask system. However, militarization of this design should be more readily accomplished than with the shadow-mask. For instance, proper control of the tensioning of the aperture grille in the vertical dimension could increase its performance under vibration and the addition of magnetic shielding should provide adequate protection against stray fields, since the convergence mechanism, for the phosphor stripes, is less critical than for the triad dot groupings.

The brightness of the Trinitron CRT is reported to be 150 fL, at conventional 525 line television scanning rates. A higher brightness is available from the Trinitron rather than from the shadow mask tube because the aperture grille intercepts fewer electrons than does the shadow mask. One could conceive of a two-color version of a Trinitron utilizing red and green as primary colors. As a consequence, a 50 percent increase in brightness would be realized resulting in a 225 fL display. Some additional increase in brightness could also be achieved by utilizing more efficient phosphors since the need to preserve the NTSC ratios, Green 59 percent and red 30 percent for the three-color CRT is not as critical. In reality, it is contrast rather than brightness that one is concerned with. In a two-color CRT using red and green as primary colors, a low pass contrast enhancement filter could be effectively utilized. Such a filter would present red and green (and combinations thereof) but not blue. At sea level, blue is not a significant portion of ambient light, however, at high altitudes, the blue (short wavelength) component of ambient light becomes appreciable. The low pass filter would effectively block the blue component of ambient light from reaching the CRT face thereby providing effective contrast enhancement.

The phosphor on the screen of the Trinitron is composed of vertical stripes of red, green and blue. The average width of these vertical stripes is 0.008 inch with 0.004 inch spacing between stripes resulting in a resolution of approximately 28 elements per inch [(0.008 + 0.004) x 3]. If a two color version was available, an effective 50 percent increase in resolution would be possible resulting in 42 elements per inch [(0.008 + 0.004) x 2].

Beam Penetration CRT

The desire to achieve color in the cockpit combined with the simplicity of construction of Color Penetration Phosphor CRT, has prompted efforts by industry to further improve the performance capability of the device. The recent introduction of a new phosphor screen, E17, (Dumont Corporation, subsidiary of Thomson – CSF), provides improved high brightness color performance.

The penetration CRT has a multilayer screen consisting of two phosphors of different colors separated by a layer of transparent dieletric material (Figure 20). The two phosphors produce different colors when excited by an electron beam. A beam of too low a voltage to penetrate the dielectric barrier layer will excite only one phosphor. Higher voltage will excite both phosphors with predominance of the second phosphor color. Intermediate colors will be obtained from intermediate voltages. Several colors can then be produced by a single electron gun by simply switching the acceleration voltage. As the acceleration voltage is switched from one value to another to produce the different colors, the current through the magnetic deflection yoke must be adjusted to keep the beam deflection amplitude constant. Also, the beam current must be modulated to keep the picture brightness constant.

Many different combinations of phosphors are possible. Practically speaking, however, for two-color presentation, they must be restricted to phosphors having equal persistance (brightness decay characteristics), good color separation, small voltage swings and good color uniformity in intermediate colors. An example of a phosphor screen developed by Dumont for cockpit displays is the E17, the characteristics of which are shown in Figures 20, 21 and 22. This screen operates with an accelerator voltage between 10 KV (red) and 17 KV (green). At 13 KV, the red and green are balanced and mix to produce yellow.

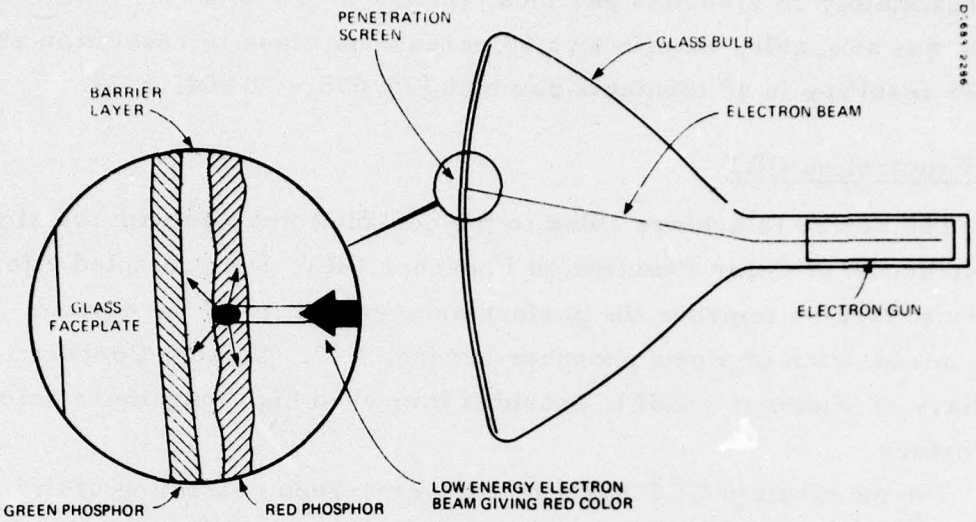

Figure 20. Color penetration CRT.

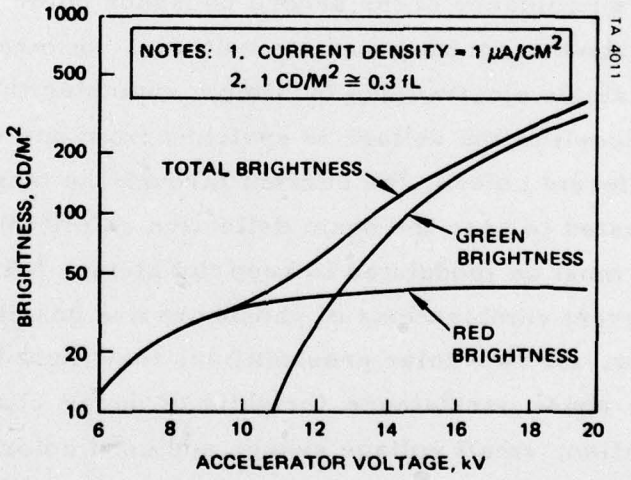

Figure 21. Relative phosphor brightness.

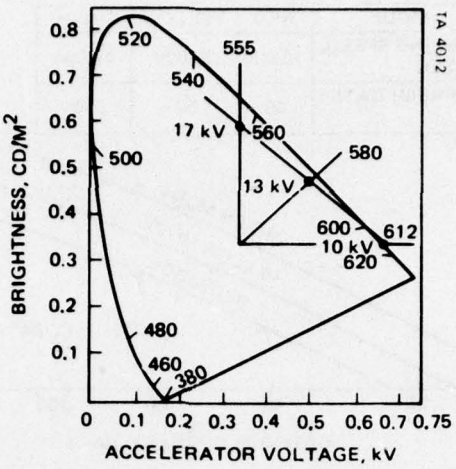

Figure 22. C.I.E. diagram for E17 penetration screen.

In determining the suitability of the penetration phosphor CRT to the highly reliable VDS application, due consideration must be given to the performance of the CRT under the actual operating conditions, namely an 875 and 525 line 60 Hz TV monitor. A serious problem in evident when considering the practicality of utilizing this type of CRT for an in-raster display. If different color symbols are required to be presented on the same TV line, the high voltage would have to be switched in a fraction of a microsecond, clearly an impossible feat due to component technology limitations. It can be argued that it is possible to separate the different colored symbols on the display and to "order" the data such as to provide adequate time to switch the high voltage. The most serious restriction of the penetration phosphor CRT appears to be its lack of adequate brightness. Figure 23 indicates that at 500 amps of beam current (a reasonable maximum) a 2000 fL line trace in the green mode and a 675 fL line trace in the red mode is achievable under the test conditions shown. This data must of course be translated to the VSD writing speed of 320,000 inches/sec in the 875 line mode at 60 Hz. In doing so, a trace brightness of 208 fL in the green mode and 18 fL in the red mode is obtained. While this represents a substantial improvement in brightness obtainable five years ago with similar CRTs, it is still far short of the 1200 fL required for the highly reliable VDS application.

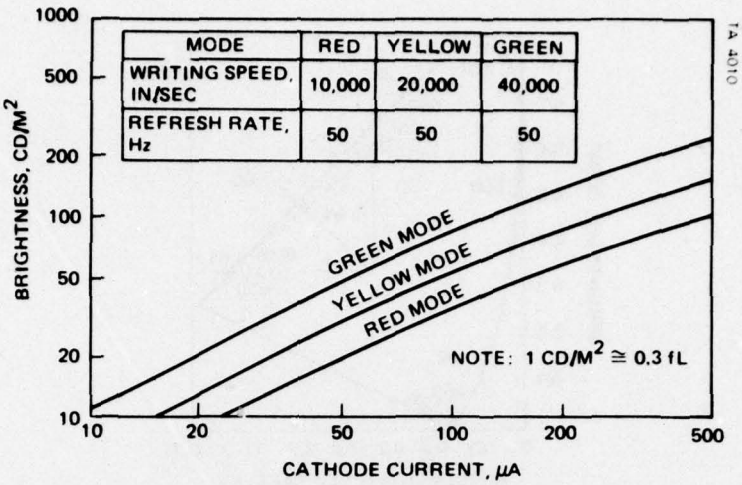

Figure 23. E17 screen trace brightness versus cathode current (through 15 percent transmission filter).

LIQUID CRYSTAL PICTORIAL DISPLAY

Introduction

A liquid Crystal Pictorial Display is currently under development by the Hughes Aircraft Company as an alternative to the conventional cathode-ray tube for the presentation of symbolic, graphic, and pictorial images for military applications. The display presents dynamic shades-of-gray television images in real time by inducing dynamic scattering in selected areas of a thin film of liquid crystal material. The material is sandwiched between a transparent conductive cover and an array of reflective electrodes formed on the surface of a semiconductor circuit substrate by metal-oxide-semiconductor (MOS) processing techniques. The area of the display is presently one-by-one-inch, and there are 10,000 picture elements (pixels) in a 100 x 100 matrix array. Recently a 2" x 2" display was fabricated and demonstrated. The 2" x 2" display was achieved by interconnecting four 1" wafers to form a quad. Figure 24 shows a TV presentation on a defect free one inch liquid crystal display.

The display was initially conceived for use as a high-resolution panel display in tactical aircraft where operation under bright daylight viewing conditions is required. Present development is also directed toward application to head-up and helmet-mounted display systems and to field-portable

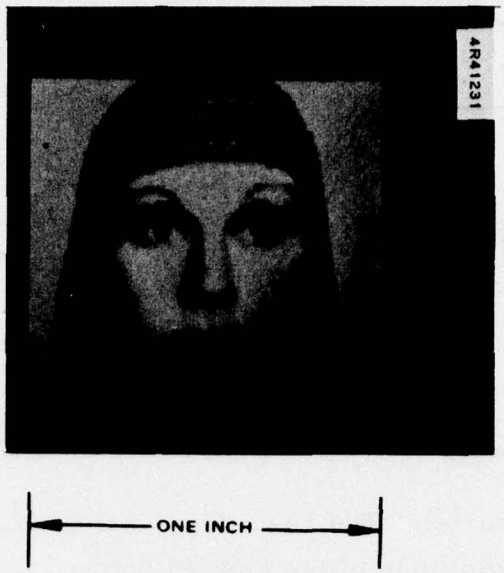

Figure 24. Defect free one inch Liquid Crystal display.

displays. Key advantages of the Liquid Crystal Pictorial Display are high contrast over small and large areas under all levels of ambient illumination, including direct sunlight; uniformly high resolution over the entire display surface; a simple electrical interface; and low weight, low power, and low installation volume. The feasibility of providing a liquid crystal color display has been demonstrated.

Electro-Optical Characteristics

A liquid crystal display, unlike a CRT, does not produce any light itself; illumination, either natural or artificial, is required. The effect of light or dark areas is produced by independent control of the diffuse reflection of incident ambient illumination from each elemental cell. Because a liquid crystal display modulates incident ambient lighting, rather than competing with it, it requires little power.

A simplified cross section of an elemental display cell is shown in Figure 25; consists of a thin film of dynamic scattering liquid crystal material sandwiched between a reflective, mirror-like electrode and a transparent conductive electrode. A voltage difference between the electrodes induces a current flow through the material which, in turn, causes hydrodynamic

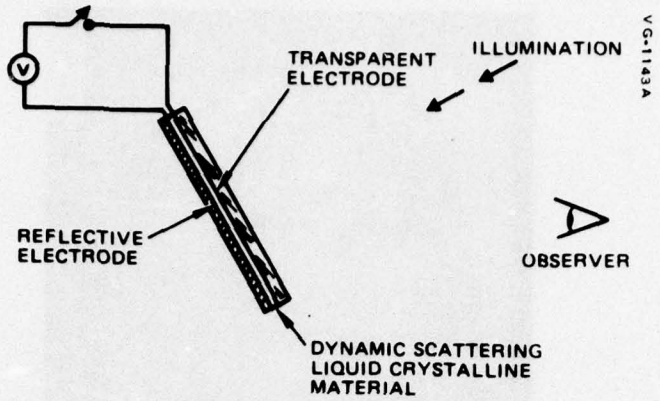

Figure 25. Reflective liquid crystal cell.

turbulence in the material. The resulting dynamic scattering is approximately proportional to the amplitude of the applied potential.

In the OFF state, with no electric potential applied to the electrode, the liquid crystal material is clear and the viewer sees whatever is specularly reflected by the display (see Figure 26a). When the display is positioned correctly with respect to a dark "light trap", the reflection of its dark surface in the electrode makes the elemental cell appear black.

In the ON state (Figure 26b) with an electric potential applied, the resulting dynamic scattering causes the display to appear a frosty white as some of the incident illumination is redirected toward the observer. Note that the illumination and the observer are on the same side of the display. Shades of gray can be obtained because the magnitude of this diffuse reflection is proportional to scattering level and, hence, to the applied potential.

The basic display is fabricated by placing the appropriate liquid crystal material between a transparent conductive electrode and the large semiconductor chip. The transparent conductive electrode is a single continuous film applied to the cover glass. The matrix array of elemental reflective electrodes that spatially define the individual pciture elements is on the surface of the semiconductor ship. Each reflective electrode serves as an electrical contact to the liquid crystal material and as an optical reflector. The film of liquid crystal material that fills the cavity between the transparent electrode and the semiconductor chip is common to the entire array of elemental reflective electrodes.

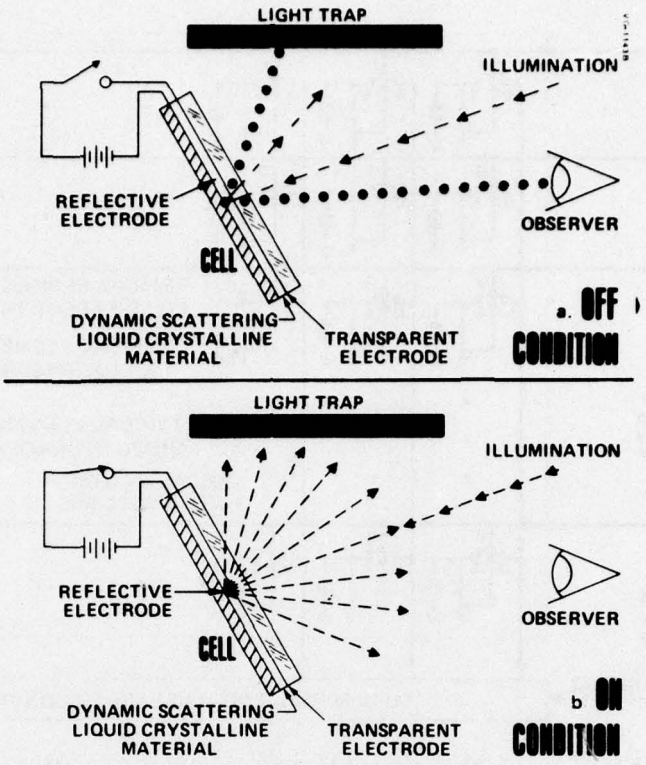

Figure 26. Liquid crystal cell operation

A circuit diagram of the addressing circuits contained within the basic electrode-array chip is shown in Figure 27. Associated with each elemental cell or picture element, is a transistor-capacitor sample-and-hold circuit and a reflective electrode.

Plans have been formulated at Hughes Aircraft Company to fabricate a liquid crystal color display by combining the liquid crystal technology and color display technology in such a way as to provide a solid state dot sequential color display. One such method involves breaking up each element of the display into a three-color triad, forming an image in the same manner as is used in the Sony Trinitron. Referring to Figure 28, a multilayer interference type color filter is placed on the inside of the cover glass, forming vertical stripes of primary color triads in registry with the elemental display cells. Since the filter will be on the side of the glass, this is in contact with the liquid crystal material, there will be negligible visual parallax. The spacing between the filter and the LX cell mirror on the backplate will be only 1/2 mil, while the filter stripe will be 10 mil wide. The filter stripes are oriented vertically.

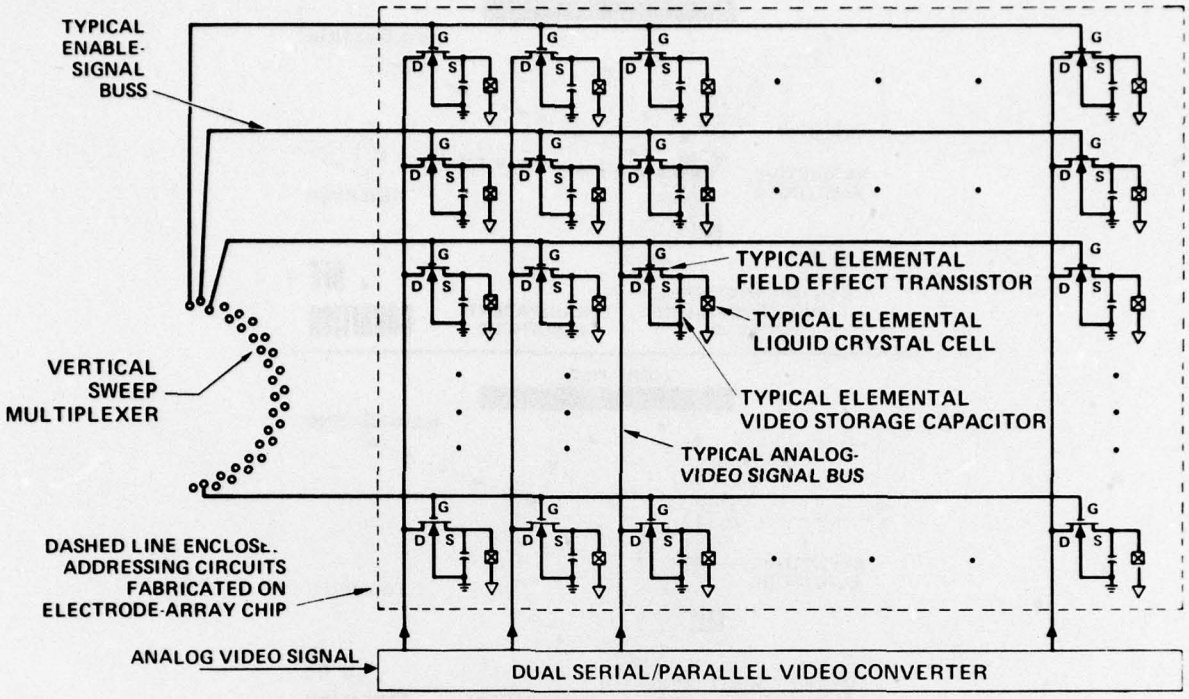

Figure 27. Liquid crystal addressing circuits.

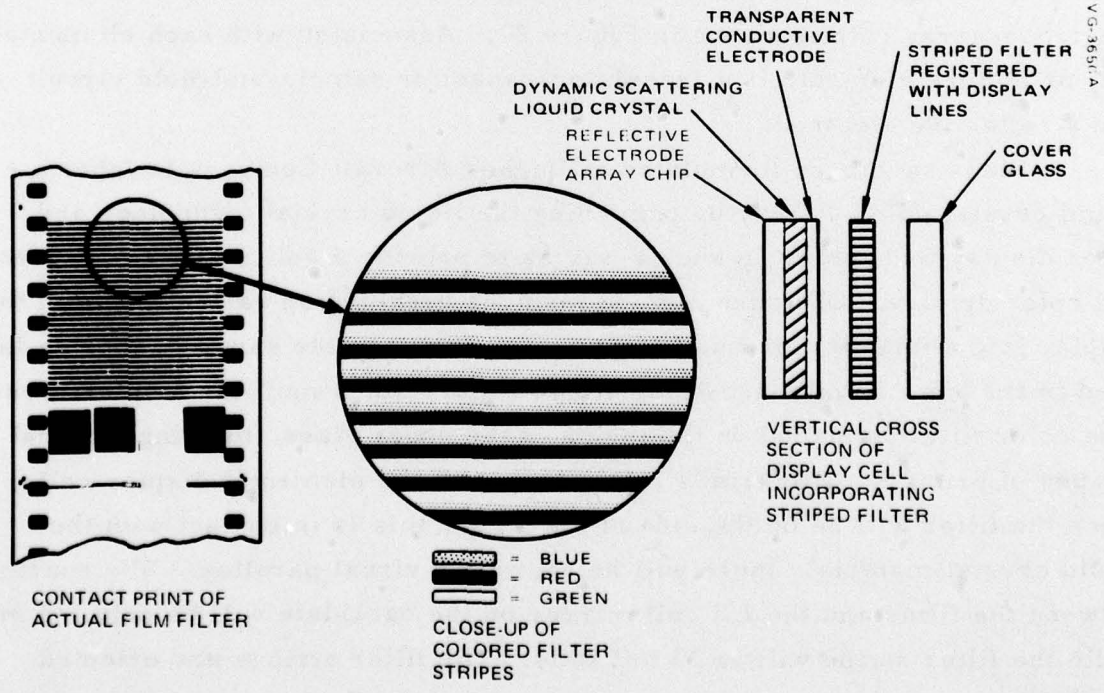

Figure 28. Color liquid crystal display mechanization.

Conclusion

During the past five years, some progress has been made by industry toward improving the brightness characteristics of color CRTs. Notable improvements have been made in the Trinitron CRT and Penetration Phosphor CRT. While these improvements are noteworthy, further order of magnitude improvements in brightness is required before these display devices can be considered for the highly reliable VSD application. For a TV raster display, the Penetration Phosphor CRT presents an additional problem, namely, the need to switch the high voltage from 17 KV to 10 KV at microsecond rates. The one display device that offers the greatest potential for providing a high brightness for both black and white and color is the Liquid Crystal Pictorial Display, currently under development. A substantial amount of further development effort, however, is required before a production version of such a display will be available.

SECTION 4
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